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Specification of high-speed transmission of DV

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Abstract:
This specification defines the packetization of a source packet, the structure of the CIP header, transmission timing for high-speed transmission of SD-DVCR, HD-DVCR and SDL-DVCR.

Keywords:
High-speed transmission, Transmission rate

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Editor, 1394 Trade Association
1111 South Main Street, Suite 122
Grapevine, TX 76051, USA

Table of contents

List of figures

1. Overview

1.1 Purpose

Purpose of this specification is to define the packet format for high-speed transmission. This is the extension to the definition in IEC 61883-2[R4], IEC 61883-3[R5], IEC 61883-5[R6].

1.2 Scope

This specification defines the packetization of a source packet, the structure of the CIP header and transmission timing for high-speed transmission that means faster than real-time transmission. It contains the specification of SD-DVCR, HD-DVCR and SDL-DVCR. Typical procedure for high-speed transmission is described in Annex.

The extension to the definition for SD-DVCR described in clause 4 will be reflected in maintenance of IEC 61883-2[R4].

The extension to the definition for HD-DVCR described in clause 5 will be reflected in maintenance of IEC 61883-3[R5].

The extension to the definition for SDL-DVCR described in clause 6 will be reflected in maintenance of IEC 61883-5[R6].

2. References

The following standards contain provisions, which through reference in this document, constitute provisions of this standard. All the standards listed are normative references. Informative references are given in Annex A. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below.

[R1] IEEE Std 1394-1995, Standard for a High Performance Serial Bus.

[R2] IEEE Std 1394a-2000, Standard for a High Performance Serial Bus – Amendment 1

[R3] IEC 61883-1, Consumer audio/video equipment – Digital interface – Part 1: General.

[R4] IEC 61883-2, Consumer audio/video equipment – Digital interface – Part 2: SD-DVCR data transmission

[R5] IEC 61883-3, Consumer audio/video equipment – Digital interface – Part 3: HD-DVCR data transmission

[R6] IEC 61883-5, Consumer audio/video equipment – Digital interface – Part 5: SDL-DVCR data transmission

[R7] TA document 2001012, AV/C Digital Interface Command Set General Specification Version 4.1

[R8] TA document 2001017, AV/C Tape Recorder/Player Subunit Specification 2.2

3. Definitions

3.1 Conformance levels

3.1.1 expected: A key word used to describe the behavior of the hardware or software in the design models *assumed* by this Specification. Other hardware and software design models may also be implemented.

3.1.2 may: A key word that indicates flexibility of choice with *no implied preference*.

3.1.3 shall: A key word indicating a mandatory requirement. Designers are *required* to implement all such mandatory requirements.

3.1.4 should: A key word indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase *is recommended*.

3.1.5 reserved fields: A set of bits within a data structure that are defined in this specification as reserved, and are not otherwise used. Implementations of this specification shall zero these fields. Future revisions of this specification, however, may define their usage.

3.1.6 reserved values: A set of values for a field that are defined in this specification as reserved, and are not otherwise used. Implementations of this specification shall not generate these values for the field. Future revisions of this specification, however, may define their usage.

NOTE —The IEEE is investigating whether the “may, shall, should” and possibly “expected” terms will be formally defined by IEEE. If and when this occurs, draft editors should obtain their conformance definitions from the latest IEEE style document.

3.2 Glossary of terms

3.2.1 byte: Eight bits of data, used as a synonym for octet.

3.2.2 CSR Architecture: A convenient abbreviation of the following reference (see clause 2): ISO/IEC 13213 : 1994 [ANSI/IEEE Std 1212, 1994 Edition], Information Technology—Microprocessor systems—Control and Status Register (CSR) Architecture for Microcomputer Buses.

3.2.3 quadlet: Four bytes of data.

3.3 Acronyms and abbreviations

AV/C Audio Video Control

IEEE The Institute of Electrical and Electronics Engineers, Inc.

4. SD-DVCR transmission

4.1 Construction of 1394 packet

4.1.1 Packetization of source packet of the SD-DVCR data stream

A source packet shall not be divided and shall be equal to a data block.

Data blocks transmitted in an IEEE 1394 isochronous cycle shall be determined according to the TR value in the CIP header (see 4.2.2). An empty packet is placed in any cycle with no data block.

Where TR value is

- 00_2 (1x), One or no data block is transmitted
- 01_2 (2x), Two or no data block are transmitted
- 10_2 (4x), Four or no data block are transmitted

The SYT field of the CIP header (see 4.2.1, 4.2.2) is used to synchronize transmitter and receiver.

4.1.2 Transmission order of video frames for high-speed transmission

Transmission order of data within one video frame is defined in IEC 61883-2[R4] Figure 1 and Figure 2. For high-speed transmission, transmission order of each video frame data shall follow the time sequence.

4.2 CIP header

4.2.1 CIP header for SD-DVCR data stream

The structure of the CIP header for the SD-DVCR data stream is conform to the two-quadlet CIP header format with SYT (see 6.2.1 of IEC 61883-1[R3]). The whole structure including the details of FDF is shown in figure 4.1. The value of FMT shall be set to 000000_2 to indicate the DVCR signal.

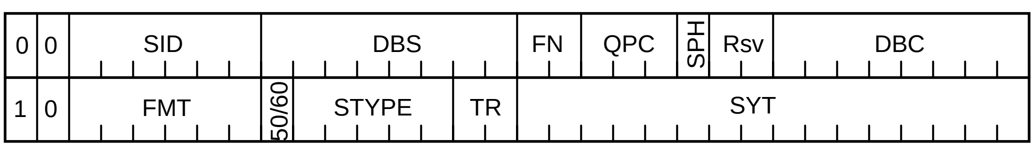

Figure 4.1 – CIP header for DVCR

4.2.2 FDF area

The Definition of the components of FDF is given as follows.

50/60 : Field system

0 = 60 field system
1 = 50 field system

STYPE : Signal type of video signal in combination with 50/60 flag as shown in table 1 of IEC 61883-2[R4].

TR : TR indicates transmission rate with following values
00_2 = 1x (normal transmission rate)
others = Defined dependent on STYPE

Where STYPE is 00000_2, TR is defined as follows.
TR : 01_2 = 2x
10_2 = 4x
11_2 = Reserved for future definition

SYT: Time stamp of video frame synchronization (see 6.2.1 of IEC 61883-1[R3])

4.2.3 DBC values

Increments of DBC value shall be determined according to the TR values.

Where TR value is
- 00_2 (1x), the DBC value increments with 1.
- 01_2 (2x), the DBC value is a multiple of 2.
- 10_2 (4x), the DBC value is a multiple of 4.

4.2.4 CIP header for 525-60 system

For the 525-60 system, the values of the CIP header components are as follows.

DBS:	01111000_2
FN:	00_2
QPC:	000_2
SPH:	0
DBC:	(see 4.2.3)
FMT:	000000_2
50/60:	0
STYPE:	00000_2
TR:	00_2 = 1x, 01_2 = 2x, 10_2 = 4x

4.2.5 CIP header for 625-50 system

For the 625-50 system, the values of the CIP header components are as follows.

DBS:	01111000_2
FN:	00_2
QPC:	000_2
SPH:	0
DBC:	(see 4.2.3)
FMT:	000000_2
50/60:	1
STYPE:	00000_2
TR:	00_2 = 1x, 01_2 = 2x, 10_2 = 4x

4.3 Transmission timing

The transmitter shall transmit a time stamp value in the SYT field once every video frame period. The time stamp should be transmitted in a packet which meets the following conditions:

− packet_arrival_time_L ≤ time stamp value

− time stamp value - transmission_delay_limit ≤ packet_arrival_time_F

where

packet_arrival_time_F is the cycle time when the first bit of the packet which has the time stamp has arrived at the receiver;

packet_arrival_time_L is the cycle time when the last bit of the packet which has the time stamp has arrived at the receiver;

transmission_delay_limit = 450 us.

In case of Hx (H = 1,2,4) transmission, KH data blocks are transmitted in a video frame period M using K isochronous packets. Isochronous packet n contains H data blocks of nH, nH+1, ... and (n+1)H-1.

The isochronous packet n of a video frame period M should be transmitted on the following conditions (n = 0, ... ,K-1):

− packet_arrival_time_L ≤ nominal timing for isochronous packet n

− nominal timing for isochronous packet n − transmission_delay_limit ≤ packet_arrival_time_F

where

packet_arrival_time_F is the cycle time when the first bit of the isochronous packet n has arrived at the receiver;

packet_arrival_time_L is the cycle time when the last bit of the isochronous packet n has arrived at the receiver;

K is the number of isochronous packets without empty packets in a video frame period.

K = 250 (525-60 system)
K = 300 (625-50 system)

Nominal timing for isochronous packet n = $T_M + (T_{M+1} - T_M) * n/K$

T_M is the time stamp for video frame period M transmitted in the SYT field.

5. HD-DVCR transmission

5.1 Construction of 1394 packet

5.1.1 Packetization of source packet of the HD-DVCR data stream

A source packet shall not be divided and shall be equal to a data block.

Data blocks transmitted in an IEEE 1394 isochronous cycle shall be determined according to the TR value in the CIP header (see 5.2.2). An empty packet is placed in any cycle with no data block.

Where TR value is

- 00_2 (1x), One or no data block is transmitted
- 01_2 (2x), Two or no data block are transmitted
- 10_2 (4x), Four or no data block are transmitted

The SYT field of the CIP header (see 5.2.1) is used to synchronize transmitter and receiver.

5.1.2 Transmission order of video frames for high-speed transmission

Transmission order of data within one video frame is defined in IEC 61883-3[R5] Figure 1 and Figure 2. For high-speed transmission, transmission order of each video frame data shall follow the time sequence.

5.2 CIP header

5.2.1 CIP header for HD-DVCR data stream

The structure of the CIP header for the HD-DVCR data stream is the same as the structure of the CIP header for the SD-DVCR data stream (see 4.2.1). The DBS for HD takes different values from that for SD through the difference of data block size as given in 4.1 of IEC 61883-3[R5].

5.2.2 FDF area

The STYPE takes different values as shown in table 1 of IEC 61883-2[R4].

Where STYPE is 00010_2, TR is defined as follows.

TR : 01_2 = 2x
10_2 = 4x
11_2 = Reserved for future definition

5.2.3 DBC values

Increments of DBC value shall be determined according to the TR value.

Where TR value is

- 00_2 (1x), the DBC value increments with 1.
- 01_2 (2x), the DBC value is a multiple of 2.
- 10_2 (4x), the DBC value is a multiple of 4.

5.2.4 CIP header for 1125-60 system

For the 1125-60 system, the values of the CIP header components are as follows.

DBS:	11110000_2
FN:	00_2
QPC:	000_2
SPH:	0
DBC:	(see 5.2.3)
FMT:	000000_2
50/60:	0
STYPE:	00010_2
TR:	00_2 = 1x, 01_2 = 2x, 10_2 = 4x

5.2.5 CIP header for 1250-50 system

For the 1250-50 system, the values of the CIP header components are as follows.

DBS:	11110000_2
FN:	00_2
QPC:	000_2
SPH:	0
DBC:	(see 5.2.3)
FMT:	000000_2
50/60:	1
STYPE:	00010_2
TR:	00_2 = 1x, 01_2 = 2x, 10_2 = 4x

5.3 Transmission timing

The transmitter shall transmit a time stamp value in the SYT field once every video frame period. The time stamp should be transmitted in a packet which meets the following conditions:

− packet_arrival_time_L ≤ time stamp value

− time stamp value - transmission_delay_limit ≤ packet_arrival_time_F

where

packet_arrival_time_F is the cycle time when the first bit of the packet which has the time stamp has arrived at the receiver;

packet_arrival_time_L is the cycle time when the last bit of the packet which has the time stamp has arrived at the receiver;

transmission_delay_limit = 450 us.

In case of Hx (H = 1,2,4) transmission, KH data blocks are transmitted in a video frame period M using K isochronous packets. Isochronous packet n contains H data blocks of nH, nH+1, ... and (n+1)H-1.

The isochronous packet n of a video frame period M should be transmitted on the following conditions (n = 0, ... ,K-1):

− packet_arrival_time_L ≤ nominal timing for isochronous packet n

− nominal timing for isochronous packet n − transmission_delay_limit ≤ packet_arrival_time_F

where

packet_arrival_time_F is the cycle time when the first bit of the isochronous packet n has arrived at the receiver;

packet_arrival_time_L is the cycle time when the last bit of the isochronous packet n has arrived at the receiver;

K is the number of isochronous packets without empty packets in a video frame period.

K = 250 (1125-60 system)
K = 300 (1250-50 system)

Nominal timing for isochronous packet n = $T_M + (T_{M+1} - T_M) * n/K$

T_M is the time stamp for video frame period M transmitted in the SYT field.

6. SDL-DVCR transmission

6.1 Construction of 1394 packet

6.1.1 Packetization of source packet of the SDL-DVCR data stream

A source packet shall not be divided and shall be equal to a data block.

Data blocks transmitted in an IEEE 1394 isochronous cycle shall be determined according to the TR value in the CIP header (see 6.2.2). An empty packet is placed in any cycle with no data block.

Where TR value is

- 00_2 (1x), One or no data block is transmitted
- 01_2 (2x), Two or no data block are transmitted
- 10_2 (4x), Four or no data block are transmitted

The SYT field of the CIP header (see 6.2.1) is used to synchronize transmitter and receiver.

6.1.2 Transmission order of video frames for high-speed transmission

Transmission order of data within one video frame is defined in IEC 61883-5[R6] Figure 1 and Figure 2. For high-speed transmission, transmission order of each video frame data shall follow the time sequence.

6.2 CIP header

6.2.1 CIP header for SDL-DVCR data stream

The structure of the CIP header for the SDL-DVCR data stream is the same as the structure of the CIP header for the SD-DVCR data stream (see 4.2.1). The DBS for SDL takes a different value from that for SD through the difference of data block size as given in 4.1 of IEC 61883-5[R6].

6.2.2 FDF area

The STYPE takes different values as shown in table 1 of IEC 61883-2[R4].

Where STYPE is 00001_2, TR is defined as follows.

TR : 01_2 = 2x
10_2 = 4x
11_2 = Reserved for future definition

6.2.3 DBC values

Increments of DBC value shall be determined according to the TR value.

Where TR value is

- 00_2 (1x), the DBC value increments with 1.
- 01_2 (2x), the DBC value is a multiple of 2.
- 10_2 (4x), the DBC value is a multiple of 4.

6.2.4 CIP header for SDL525-60 system

For the SDL525-60 system, the values of the CIP header components are as follows.

DBS: 00111100_2
FN: 00_2
QPC: 000_2
SPH: 0
DBC: (see 6.2.3)
FMT: 000000_2
50/60: 0
STYPE: 00001_2
TR: 00_2 = 1x, 01_2 = 2x, 10_2 = 4x

6.2.5 CIP header for SDL625-50 system

For the SDL625-50 system, the values of the CIP header components are as follows.

DBS: 00111100_2
FN: 00_2
QPC: 000_2
SPH: 0
DBC: (see 6.2.3)
FMT: 000000_2
50/60: 1
STYPE: 00001_2
TR: 00_2 = 1x, 01_2 = 2x, 10_2 = 4x

6.3 Transmission timing

The transmitter shall transmit a time stamp value in the SYT field once every video frame period. The time stamp should be transmitted in a packet which meets the following conditions:

− packet_arrival_time_L ≤ time stamp value

− time stamp value - transmission_delay_limit ≤ packet_arrival_time_F

where

packet_arrival_time_F is the cycle time when the first bit of the packet which has the time stamp has arrived at the receiver;

packet_arrival_time_L is the cycle time when the last bit of the packet which has the time stamp has arrived at the receiver;

transmission_delay_limit = 450 us.

In case of Hx (H = 1,2,4) transmission, KH data blocks are transmitted in a video frame period M using K isochronous packets. Isochronous packet n contains H data blocks of nH, nH+1, ... and (n+1)H-1.

The isochronous packet n of a video frame period M should be transmitted on the following conditions (n = 0, ..., K-1).

− packet_arrival_time_L ≤ nominal timing for isochronous packet n

− nominal timing for isochronous packet n − transmission_delay_limit ≤ packet_arrival_time_F

where

packet_arrival_time_F is the cycle time when the first bit of the isochronous packet n has arrived at the receiver;

packet_arrival_time_L is the cycle time when the last bit of the isochronous packet n has arrived at the receiver;

K is the number of isochronous packets without empty packets in a video frame period.

K = 250 (SDL 525-60 system)
K = 300 (SDL 625-50 system)

Nominal timing for isochronous packet n = $T_M + (T_{M+1} - T_M) * n/K$

T_M is the time stamp for video frame period M transmitted in the SYT field.

7. Annexes

Annex A: : Procedure for high-speed transmission (informative)

A.1 General

This annex provides a guideline for command based high-speed transmission between a source device and a destination device.

Devices which support high-speed transmission should implement INPUT PLUG SIGNAL FORMAT control and OUTPUT PLUG SIGNAL FORMAT control command defined in AV/C Digital Interface Command Set General Specification[R7] to configure a serial bus input plug and a serial bus output plug to the designated format.

Examples of typical procedure for high-speed transmission are described as follows.

A.2 Examples of typical procedure

A.2.1 Example 1

A controller is embedded in a destination device as shown in Figure A.1.

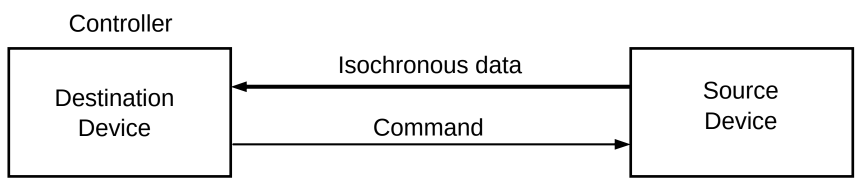

Figure A.1 – Data flow when a controller is embedded in a destination device

1) Inquiry of command implementation

A controller checks if a source device implements OUTPUT PLUG SIGNAL FORMAT control command using SPECIFIC INQUIRY command. The controller can confirm the source device implements the corresponding transmission rate by setting the TR bits in the FDF to values other than 00_2. If the source device responses IMPLEMENTED, then the following procedure is proceeded.

Note: INQUIRY from the controller is not necessary for every event. Once implementation is confirmed, this step can be skipped.

2) Configure serial bus output plug

A controller configures a serial bus output plug of a source device using OUTPUT PLUG SIGNAL FORMAT control command. For example, when the controller makes the source device set in high-speed transmission, the controller uses OUTPUT PLUG SIGNAL FORMAT control command where the TR bits in the FDF has values other than 00_2

3) Establish connections

A connection between a source device and a destination device is established according to the procedure described in IEC61883-1[R3].

4) Start high-speed reproduction

A controller instructs a source device to start high-speed reproduction using PLAY control command with FORWARD playback mode defined in AV/C Tape Recorder/Player Subunit Specification[R8]. When the command is ACCEPETD, the source device starts to reproduce and transmit data in the transmission rate that has been configured by the OUTPUT PLUG SIGNAL FORMAT control command.

5) Stop high-speed reproduction

A controller instructs a source device to stop high-speed reproduction using WIND control command with STOP subfunction defined in AV/C Tape Recorder/Player Subunit Specification[R8]. This command does not affect the configuration of serial bus output plug.

A.2.2 Example 2

A controller is embedded in a source device as shown in Figure A.2

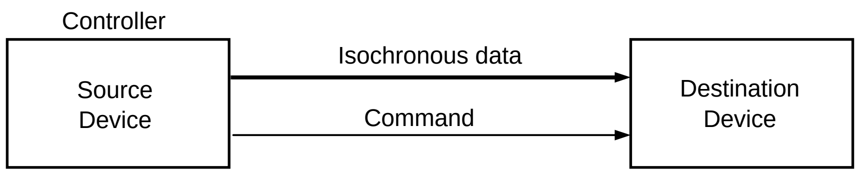

Figure A.2– Data flow when a controller is embedded in a source device

1) Inquiry of command implementation

A controller checks if a destination device implements INPUT PLUG SIGNAL FORMAT control command using SPECIFIC INQUIRY command. The controller can confirm the destination device implements the corresponding transmission rate by setting the TR bits in the FDF to values other than 00_2. If the destination device responses IMPLEMENTED, then the following procedure is proceeded.

Note: INQUIRY from controller is not necessary for every event. Once implementation is confirmed, this step can be skipped.

2) Configure serial bus input plug

A controller configures a serial bus input plug of a destination device using INPUT PLUG SIGNAL FORMAT control command. For example, when the controller makes the destination device set in high-speed transmission, the controller uses INPUT PLUG SIGNAL FORMAT control command where the TR bits in the FDF has values other than 00_2.

3) Establish connections

A connection between a source device and a destination device is established according to the procedure described in IEC61883-1 [R3].

4) Start high-speed recording

A controller instructs a destination device to start high-speed recording using RECORD control command with RECORD recording mode defined in AV/C Tape Recorder/Player Subunit Specification[R8]. When the command is ACCEPTED, the destination device starts to record an incoming data in the transmission rate that has been configured by the INPUT PLUG SIGNAL FORMAT control command.

5) Stop high-speed recording

A controller instructs a destination device to stop high-speed recording using WIND control command with STOP subfunction.