



Document number 2006019

Networking IEEE 1394 Clusters via UWB
over Coaxial Cable- Part 1: Continuous
Pulse (C-UWB) PHY

June 29, 2007

Accepted for publication by

The 1394 Trade Association Board of Directors has accepted this technical specification

Abstract

This technical specification defines a continuous pulse UWB physical layer (C-UWB PHY) that is suitable to interconnect clusters of IEEE 1394 devices via coaxial cable transmission line networks.

Keywords

C-UWB, coaxial cable, IEEE 802.15.3, IEEE 1394, Serial Bus

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Published by:

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Foreword

This technical specification defines Part 1: C-UWB PHY of suite of documents specifying the networking IEEE 1394 clusters via UWB over coaxial cable.

The Board of Directors of the 1394 Trade Association accepted this technical specification on June 29, 2007. Board of Directors acceptance of this technical specification does not necessarily imply that all board members voted for acceptance. At the time the 1394 Trade Association Board of Directors accepted this technical specification, it had the following members:

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 Zeph Freeman, *Vice Chair*
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 Jalil Oraee, *Finance*
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 Mark Slezak
 Dave Thompson, *Secretary*
 Hans van der Ven

The following organizations were represented in the Wireless Working Group:

Agere Systems	Newnex Technologies
AV Connections	Oxford Semiconductor
Congruent Software	Pulse~LINK
Electronic Links	Quantum Parametrics
Fraunhofer IPMS	Samsung
Feescale Semiconductor	Texas Instruments
Microsoft	The Powers.net
	WJR Consulting

The Wireless Working Group, which developed and reviewed this technical specification, had contributions from the following members:

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Networking IEEE 1394 Clusters via UWB over Coaxial Cable-

Part 1: Continuous Pulse (C-UWB) PHY

Scope and purpose

1.1 Scope

The scope of this technical specification is to define a Continuous Pulse Ultra-wideband (C-UWB) physical layer (PHY) that together are suitable to interconnect clusters of IEEE 1394 devices *via* coaxial cable transmission line networks.

1.2 Purpose

IEEE 1394 is a cost-effective interconnect for two important groups of devices: desktop and notebook computers and their associated peripherals on the one hand and consumer electronic devices on the other. IEEE 1394 is increasingly a convergent interconnect between the two groups. However, the use of IEEE 1394 in other environments, *e.g.*, the transfer of high-speed digital video data between rooms of a house, is hampered by the lack of network technologies that are both commercially viable and support the quality of service necessary for demanding high-definition audio and video streams. This technical specification provides the foundation for pragmatic and readily deployable solutions because it leverages existing and widespread residential coaxial cable transmission line networks. The cardinal goal has been to enable a larger market for IEEE 1394 products with a technically solid solution that is also pragmatic and readily deployable.

2 Normative references

2.1 Reference scope

The specifications and standards named in this section contain provisions which through reference in this text, constitute provisions of this 1394 Trade Association Technical Specification. At the time of publication, the editions indicated are valid. All specifications and standards are subject to revision; parties to agreements based on this 1394 Trade Association Technical Specification are encouraged to investigate the possibility of applying the most recent editions of the specifications and standards indicated below.

2.2 Approved references

The following approved specifications and standards may be obtained from the organizations that control them.

- [R1] IEEE Std 802.15.3-2003, Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Wireless High Rate Personal Networks
- [R2] IEEE Std 802.15.3b-2005, Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Wireless High Rate Personal Networks—Amendment 1: MAC Sublayer

Throughout this document, the term “IEEE 802.15.3” shall be understood to refer to IEEE Std 802.15.3-2003 as amended by IEEE Std 802.15.3b-2005.

2.3 Reference acquisition

The references cited may be obtained from the organizations that control them:

1394 Trade Association, 315 E Lincoln, Suite E, Mukilteo, WA 98275 USA; (817) 410-5750 / (817) 410-5752 (FAX); <http://www.1394ta.org/>

Institute of Electrical and Electronic Engineers (IEEE), 445 Hoes Lane, PO Box 1331, Piscataway, NJ 08855-1331, USA; (732) 981-0060 / (732) 981-1721 (FAX); <http://www.ieee.org/>

3 Definitions and notation

3.1 Definitions

3.1.1 Conformance

Several keywords are used to differentiate levels of requirements and optionality, as follows:

expected: A keyword used to describe the behavior of the hardware or software in the design models assumed by this technical specification. Other hardware and software design models may also be implemented.

ignored: A keyword that describes bits, bytes, quadlets, octlets or fields whose values are not checked by the recipient.

may: A keyword that indicates flexibility of choice with no implied preference.

reserved: A keyword used to describe objects (bits, bytes, quadlets, octlets and fields) or the code values assigned to these objects in cases where either the object or the code value is set aside for future standardization. Usage and interpretation may be specified by future extensions to this or other specifications and technical specifications. A reserved object shall be zeroed or, upon development of a future specification or technical specification, set to a value specified by such a specification or technical specification. The recipient of a reserved object shall ignore its value. The recipient of an object defined by this technical specification as other than reserved shall inspect its value and reject reserved code values.

shall: A keyword that indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to assure interoperability with other products conforming to this technical specification.

should: A keyword that denotes flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “is recommended.”

3.1.2 Glossary

The following terms and specific values are used in this technical specification:

binary phase shift keying: UWB pulse-polarity modulation; a modulation method wherein the transmitted polarity, (+1) or (−1), of UWB pulses encodes a symbol, and further where the symbol polarity encodes the data bit value. Insofar as there is no phase to shift in UWB, the terminology is a holdover from the analogous conventional radio modulation method.

chip rate: The fixed rate at which UWB pulses are sent. The nominal chip rate in this specification is 1.35 Gc/s

coaxial cable: Unbalanced transmission line used in CATV installations.

processing gain: Defined as Symbol Duration/Chip Duration. This specification defines operating modes with processing gains of 1, 2, 4, 8, or 64.

pulse: An emitted signal whose duration is equal to the reciprocal of the ultra-wideband 3-dB bandwidth. In pulsed UWB, pulse is synonymous with chip. The nominal chip duration in this specification is 740.74 ps.

quadrature phase shift keying: A modulation method wherein two synchronized streams of orthogonal UWB pulses, each independently polarity modulated, are sent simultaneously with voltage signals added. Insofar as there is no phase to shift in UWB pulses, the terminology is a holdover from the analogous conventional radio modulation method.

splitter: A coaxial cable device with one input port and multiple output ports; the input signal(s) are replicated on, and power divided among the output ports while maintaining nominal coaxial line impedance.

Golay spreading code: Golay codes are sets of orthogonal binary sequences. Length n Golay codes are used for spreading. In this specification n shall take on values of 1 (no code), 2, 4, 8, 64 or 128. The notation for a Golay code sequence of length n is G_n .

symbol: A representation of a single data bit. Symbols are mapped onto contiguous sequences of chips. Symbol length varies according to processing gain; a symbol may map to 2, 4, 8 or 64 chips.

3.1.3 Abbreviations

The following abbreviations are used in this technical specification:

AGC	Automatic gain control
$b_0:b_N$	The set of numbers $b_0, b_1, b_2, \dots, b_N$
BcstID	Broadcast identifier
BPSK	Binary phase shift keying (in UWB, pulse polarity modulation)
CATV	Community Access Television (<i>i.e.</i> , cable television)
CCA	Clear channel assessment
C-UWB	Continuous pulse UWB
DestID	Destination identifier
DEVID	Device identifier
FCSL	Frame convergence sublayer
FEC	Forward error correction
Gc/s	Giga-chips per second
G_N	Golay code of length N
HCS	Header check sequence
ITU	International Telecommunications Union
ITU-R	International Telecommunications Union (Radio Communications)
LDPC	Low-density parity check
LLC	Logical link control
MAC	Medium access control
Mb/s	Megabits per second
Mc/s	Mega-chips per second
MS/s	Mega-symbols per second
MSDU	MAC service data unit
MSO	Multiple service operator
OUI	Organizationally unique identifier
PG	Processing gain, the ratio of symbol duration to chip duration
PHY	Physical layer
PIB	Piconet Information Base
PLCP	Physical layer convergence protocol
PNC	Piconet coordinator
PPDU	PHY Protocol Data Unit
PRBS	Pseudo-random bit sequence
PSDU	Physical layer service data unit
QPSK	Quadrature phase shift keying (in UWB, polarity-modulation of orthogonal pulses)
RF	Radio frequency
RSP	Reservation service provider
SNAP	Sub-network access protocol
SrcID	Source identifier
UWB	Ultra-wideband

3.2 Numeric Values

Decimal and hexadecimal numbers are used within this specification. By editorial convention, decimal numbers are most frequently used to represent quantities or counts. Addresses are uniformly represented by hexadecimal numbers. Hexadecimal numbers are also used when the value represented has an underlying structure that is more apparent in a hexadecimal format than in a decimal format.

Decimal numbers are represented by Arabic numerals without subscripts or by their English names. Hexadecimal numbers are represented by digits from the character set 0 – 9 and A – F followed by the subscript 16. When the subscript is unnecessary to disambiguate the base of the number, it may be omitted. For the sake of legibility, hexadecimal numbers are separated into groups of four digits separated by spaces.

As an example, 42 and $2A_{16}$ both represent the same numeric value.

4 Physical (PHY) layer

4.1 Overview

This clause specifies Continuous Pulse UWB (C-UWB) physical layer (PHY) protocols and signaling for high-speed data transmission over coaxial cable. Signaling is polarity modulated at a rate of 1350 Mc/s. Different transmission modes derive from the effect of spread factors and forward error correction (FEC) on the underlying signaling rate; the resultant data rates range from 21 Mb/s to 2700 Mb/s inclusive.

The C-UWB PHY's characteristics are tailored to residential coaxial cable networks. The C-UWB PHY operates in coexistence-compatible spectrum by transmitting specially designed UWB pulses in coded sequences. To avoid interference with existing and contemplated CATV signals, the C-UWB PHY is constrained to a bandwidth of 1.35 GHz centered at 4.05 GHz.

4.2 Transmitter and receiver functional components

The C-UWB PHY Technology top-level description is shown in Figure 1. In the transmitter, the PPDU data are scrambled, encoded, spread and formatted, then mapped into symbols and modulated onto the final waveform for transmission over the cable system. Upon reception, the waveform is de-modulated, and the chip stream is de-spread, decoded and de-scrambled for presentation to the MAC. Dataflow in the transmitter and receiver are illustrated by Figure 1.

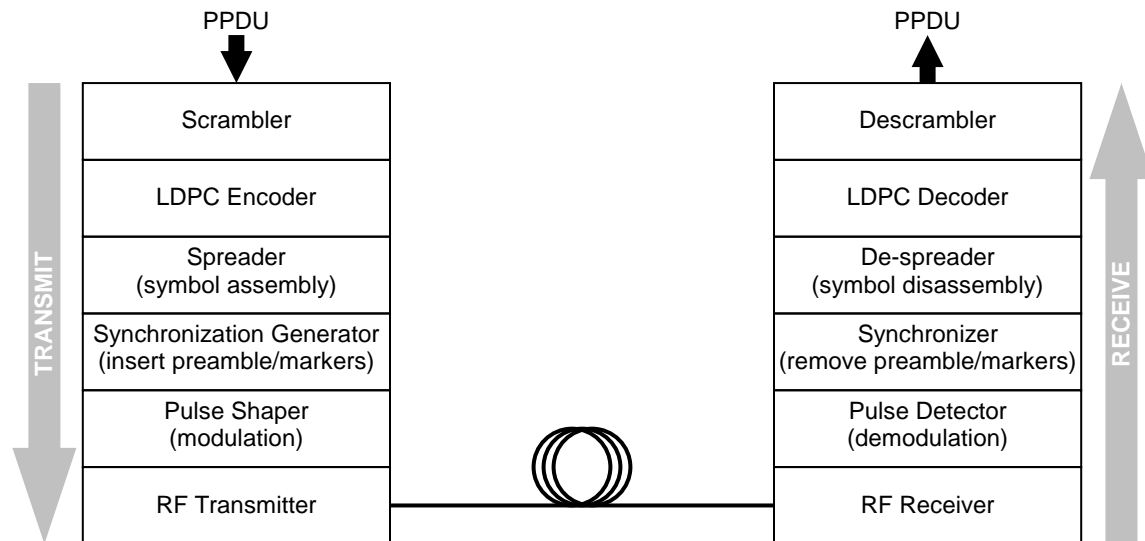


Figure 1 – C-UWB PHY transmitter and receiver dataflow

A chip (or pulse) is the fundamental C-UWB PHY signaling unit and is transmitted at a fixed rate of 1.35 Gc/s for either one pulse shape or a parallel pair of orthogonal pulses. Parallel sequences of chips using orthogonal UWB pulses double the combined chip rate to 2.7 Gc/s. The information content of a sequence of chips varies according to the FEC rate, the spread factor, and the pulse orthogonality.

The first transformation applied to the input bit stream is scrambling. Then forward error correction (FEC) using Low Density Parity Check (LDPC) algorithm is applied to the scrambled bits. The number of output bits (coded bits) varies according to the inverse of the FEC rate, *e.g.*, for an FEC rate of $2/3$, three bits are output for every two bits input.

Next, this encoded bit stream is then "spread" by the spreading code sequence. Spreading is defined by performing a dot-multiplication (<.>) of each information bit by a contiguous set of chips that are chosen based on a given spreading code sequence. In other words, if the encoded bit is +1, the spreading code sequence is transmitted without change in the polarity, and if the encoded bit is -1, the spreading code sequence is transmitted in the opposite polarity. The result of this multiplication are symbols, S, which comprise contiguous sets of 1, 2, 4, 8 or 64 encoded chips. The ratio of the symbol duration (in time) to the chip duration (in time) is called the processing gain, PG.

Finally, symbols are polarity encoded before transmission over the coax media. Polarity encoding is also referred to as Binary Phase-Shift keying (BPSK). Optionally sequences of two orthogonal UWB pulses comprise symbols and are referred to as Quadrature Phase-Shift Keying (QPSK) When BPSK is used the chip values of +1 or -1 determine the transmitted polarity of the chip (pulse). QPSK modulation doubles the effective data rate by concurrently transmitting two independent BPSK-encoded data streams via orthogonal pulses. The terms BPSK and QPSK are loosely analogous to the same terms used in conventional carrier-based modulations.

In the receive process the exact mirror image steps are followed to convert the received chips back to the information bits.

4.3 PPDU frame format

Figure 2 shows the format for the PPDU frame, which is composed of three major components: the PPDU preamble, the frame header (PHY header, scrambled MAC header, scrambled header check sequence), and the MAC frame body (frame payload plus FCS).

In creating a frame for transmission, the PHY pre-appends the PHY header to the MAC header and then calculates the HCS over the combined headers. The resulting HCS is appended to the end of the MAC header. The PPDU preamble is first, followed by the frame header, followed by the frame payload and finally the FCS. The remainder of the PPDU frame, *i.e.*, the data field (frame payload and FCS), is transmitted at the desired information data rate (see Table 1).

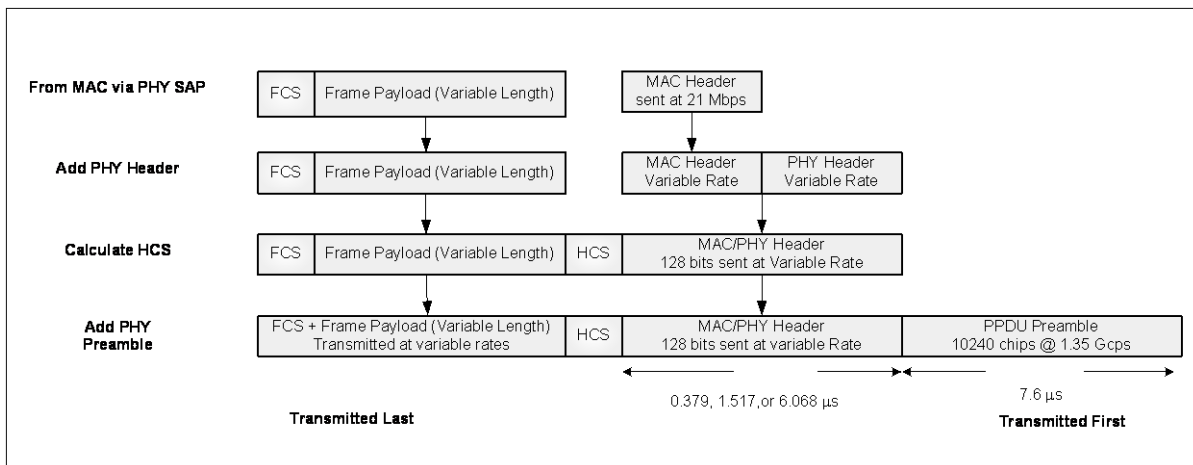


Figure 2 – PPDU frame format

4.3.1 PPDU encoding

The encoding process is composed of many steps as illustrated in Figure 1. These steps are fully described in later clauses, as noted below. The following intends to facilitate understanding the details described in the subsequent clauses:

- The PHY header field is produced from the LENGTH, SEEDID, and RATE fields, as described in 4.5.1, and prepends the PHY layer to the MAC header, as described in 4.5.

- b) As described in 4.5.3, the HCS is calculated over the combined PHY and MAC headers, and is appended to the end of the MAC header.
- c) The scrambler is initiated according to the SEEDID field, as provided in 4.5.1.2, generates a scrambling sequence which is XOR combined with the content of the MAC header, HCS, frame payload, and FCS fields. The PHY header shall not be scrambled.
- d) The frame header is spread by a length 4, 16, or 64 spreading sequence, and the data field is spread by a mode-dependent length 1, 2, 4, 8, or 64 spreading sequence as described in 4.10.
- e) The PPDU preamble field is produced from the SYNC field (used for AGC, diversity selection, timing acquisition, and coarse frequency acquisition and channel estimation in the receiver), and SFD field (used to indicate the start of the frame), as described in 4.4. The PPDU preamble field is pre-appended to the frame header and is based on length 128 Golay symbols.
- f) Marker symbols (used for channel, timing and frequency tracking) are based on length 128 Golay symbols that are inserted periodically every 24,576 chips in the frame body field as described in 0.
- g) The frame header is modulated in the base rate BPSK mode and the data field is modulated using BPSK/QPSK at the rate specified in the RATE field in the header. For the mandatory mode, the base rate shall be nominally 21 MS/s as specified in Table 1.

4.3.2 PPDU rate-dependent parameters

Table 1 specifies PPDU rate dependent parameters; mandatory operating modes are shaded in gray.

Table 1 – PPDU rate-dependent parameters

Transmit Rate	Data Rate (Mb/s)	FEC Factor	Spread Factor	Modulation	Mandatory
1	1350	1	1	BPSK	
2	900	2/3	1	BPSK	
3	675	1/2	1	BPSK	Yes
4	450	2/3	2	BPSK	
5	338	1/2	2	BPSK	Yes
6	225	2/3	4	BPSK	
7	169	1/2	4	BPSK	Yes
8	113	2/3	8	BPSK	
9	84	1/2	8	BPSK	Yes
10	21	1	64	BPSK	Yes
11	2700	1	1	QPSK	
12	1800	2/3	1	QPSK	
13	1350	1/2	1	QPSK	
14	900	2/3	2	QPSK	
15	675	1/2	2	QPSK	
16	450	2/3	4	QPSK	
17	338	1/2	4	QPSK	
18	225	2/3	8	QPSK	
19	169	1/2	8	QPSK	

20	42	1	64	QPSK	
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4.3.3 PPDU timing parameters

Table 2 lists the timing parameters associated with the PPDU.

Table 2 – PPDU timing parameters

Parameter	Value	Units	Description
R_{chip}	1350	MHz	Chip rate
T_{chip}	740.74	ps	Chip duration
N_{psym}	10240	chips	PPDU preamble symbol length ($80 \times G_{128}$)
T_{psym}	7.585	μ s	PPDU preamble symbol duration
N_{sync}	76	G_{128} symbols	SYNCHfield size
T_{sync}	7.2065	μ s	SYNCH field duration
N_{sfd}	4	G_{128} symbols	SFD field size
T_{sfd}	0.379	μ s	SFD field duration
N_{mhdr}	128	bits	PHY/MAC header size
T_{mhdr}	0.379 1.517 6.068	μ s	PHY/MAC header duration
N_{phdr}	32	bits	PPDU header size
N_{mhdr}	80	bits	MSDU header size
N_{marker}	1152	chips	Marker size ($9 \times G_{128}$)
T_{marker}	853.3	ns	Marker duration
N_{hdrc}	16	bits	HCS size
T_{hdrc}	0.759	μ s	HCS duration
N_{block}	24576	chips	Block size
T_{Block}	18.2 μ s	μ s	Block duration
N_{dsym}	1 2 4 8 64	chips	Data symbol size

4.4 PPDU preamble

A PPDU preamble shall be added prior to the frame header to aid receiver algorithms related to AGC setting, timing acquisition, coarse frequency recovery, packet and frame synchronization, and channel estimation.

The PPDU preamble shall be transmitted at the base rate. The mandatory base rate is 21 MS/s.

Figure 3 shows the structure of the PPDU preamble. The preamble can be sub-divided into two distinct portions: a packet synchronization sequence (SYNC), a frame delimiter sequence (SFD). The durations of these portions are provided in Table 2. These following clauses detail the different portions of the preamble.

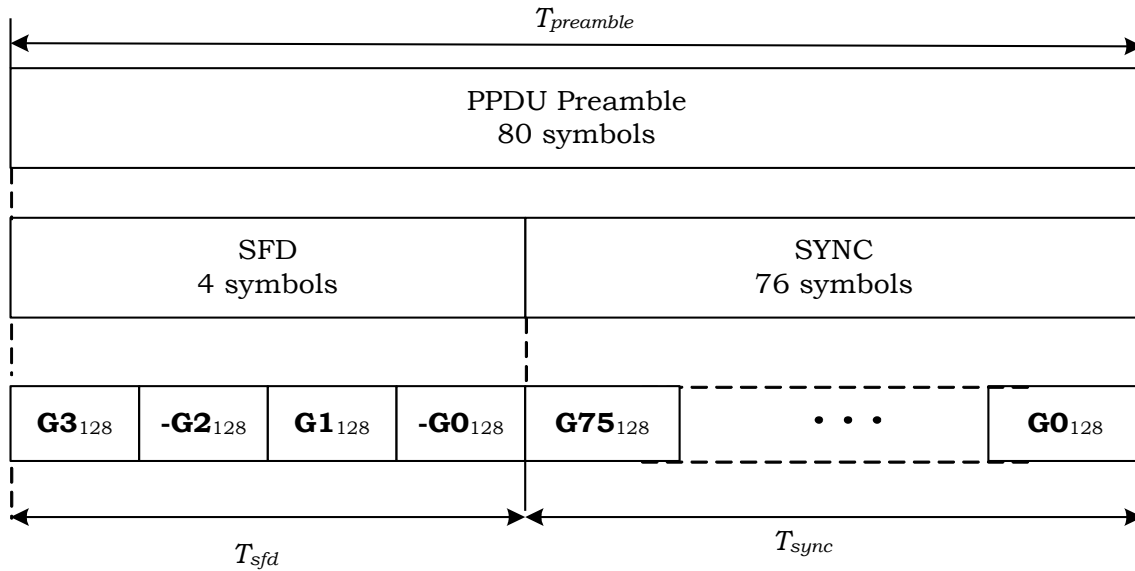


Figure 3 – PPDU preamble structure

4.4.1 PPDU synchronization (SYNC) field

The SYNC field shall consist of N_{SYNC} symbols of ones spread by G_{128} (Golay Code of length 128), as defined in

Table 9. The number of symbols, N_{SYNC} , is 76. This field shall be provided so that the receiver can perform the necessary operations for frame synchronization.

Note: The notation Gn_{128} is used to designate the n th symbol of the SYNC field that is spread by G_{128} .

4.4.2 PPDU start frame delimiter (SFD) field

SFD shall be provided to establish frame timing. The SFD shall be encoded as $[-1 +1 -1 +1]$ and spread by G_{128} , where the leftmost bit shall be transmitted first.

Note: The notation Gx_{128} is used to designate the x th symbol of the SFD field that is spread by G_{128} .

4.5 Frame header

A frame header, shown in Figure 4, shall be added after the PPDU preamble. It conveys information in the PHY and the MAC headers necessary for a successful decoding of the packet.

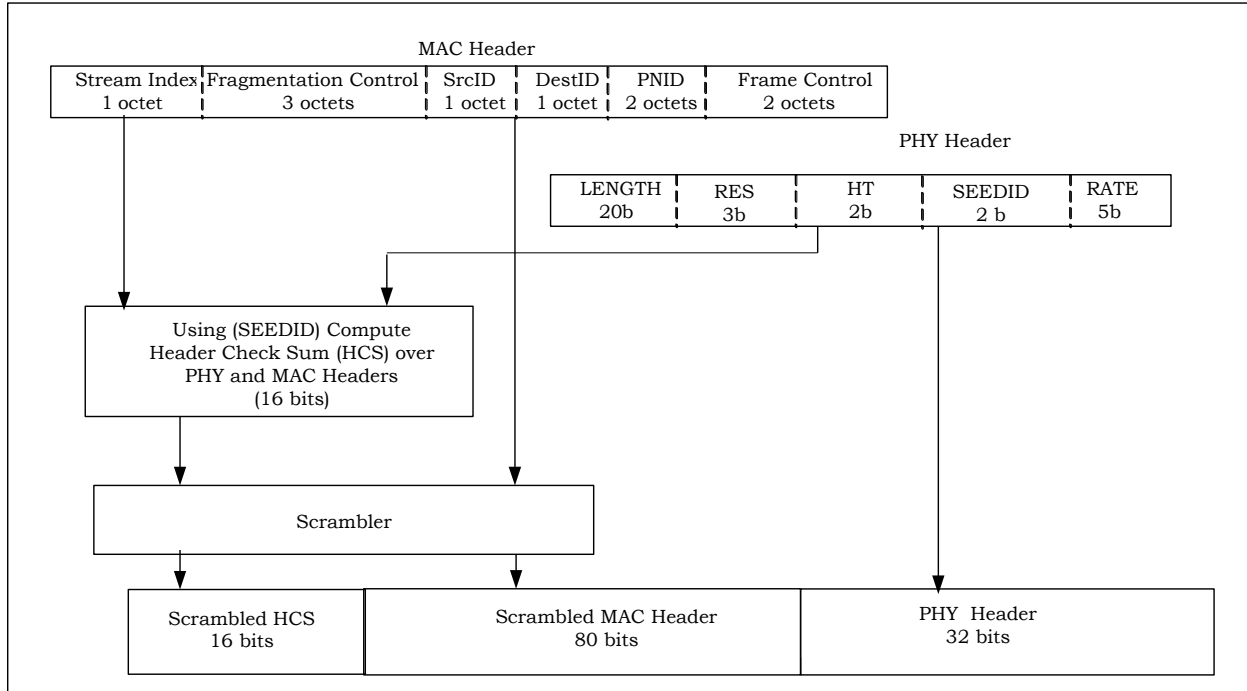


Figure 4 – Frame header and HCS flow diagram

4.5.1 PHY header

The PHY header contains information about the length of the frame payload, the seed identifier for the scrambler, and the data rate of the data field.

The PHY header field shall consist of 32 bits, as illustrated in Figure 5. There are 3 reserved bits for future use and shall be set to zero. The rest of the fields are described below.

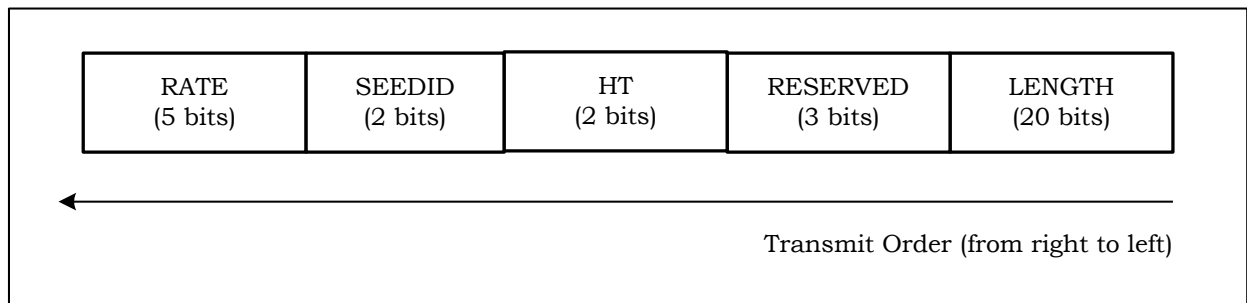


Figure 5 – PHY header bit assignment

4.5.1.1 PPDU length (LENGTH) field

The PPDU length field shall be an unsigned 20-bit integer number that indicates the number of octets in the frame payload (which does not include the FCS) that the MAC is currently requesting the PHY to transmit.

4.5.1.2 PPDU scrambler (SEEDID) field

The MAC shall set bits S1-S2 according to the scrambler seed identifier value as shown in Table 4. This 2-bit value corresponds to the seed value chosen for the data transfer.

4.5.1.3 PPDU transmit mode (RATE) field

The MAC shall set the RATE field (bits R1 - R5) to a transmit mode value specified by Table 1. The transmit mode specifies FEC factor, spread factor and modulation scheme—which, in turn, yield the transmit rate.

4.5.1.4 Header type (HT) field

Header type field specifies the spread factor applied to the header field. A 2-bit field shall be set to values specified in Table 3.

Table 3 -- HT field

Value	Header Spread Factor
0	64
1	16
2	4
3	Reserved

4.5.2 MAC header

The 80-bit MAC header is specified by IEEE 802.15.3 (see [R1] [R2]).

4.5.3 Header check sequence

The combination of PHY header and the MAC header shall be protected with an ITU-T CRC-16 header check sequence (HCS) as specified by IEEE 802.15.3. (see [R1]).

4.6 Data field

The Data field is the last component of the PPDU, and is encoded as shown in Figure 7.

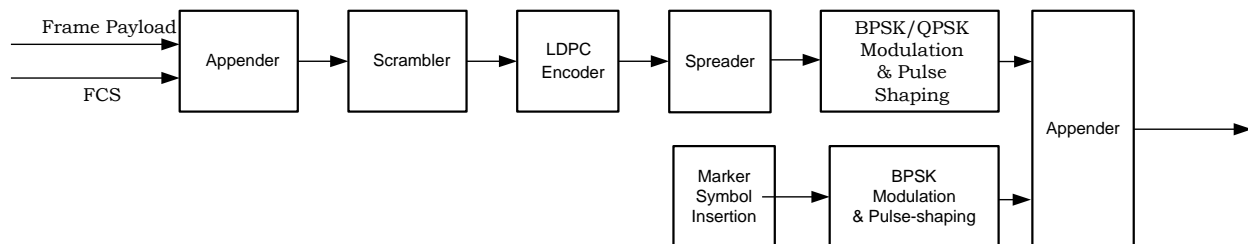


Figure 6 – Data field encoding process

The data field shall be formed as follows:

- a) Form the non-scrambled data field by appending the frame load with the FCS;

- b) Scramble the resulting combination according to 4.7;
- c) Encode the scrambled data field using FEC code as described in 4.8;
- d) Spread the encoded and scrambled data field using a spreading code of length 1, 2, 4, 8, or 64 as detailed in 4.10.1;
- e) Insert marker symbols into the resulting data field according to 4.10.2; and
- f) Map the data field onto BPSK/QPSK symbols. Marker Symbols shall be mapped to ONLY BPSK symbols.

4.7 Scrambler

As specified in [R1], the input data shall be scrambled by modulo-2 addition of the data with the output of a pseudorandom number generator, as illustrated in Figure 7.

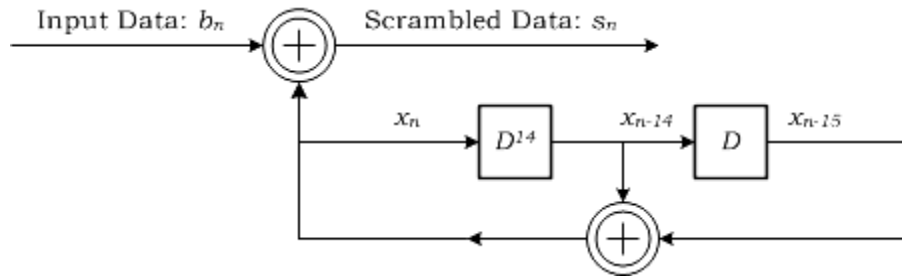


Figure 7 – Data scrambling via a linear feedback shift register

The scrambler shall be used for the MAC header, HCS, frame body, and FCS. The PHY preamble, PHY header, and RSP shall not be scrambled. The polynomial (1) for the pseudorandom number generator used by the scrambler shall be:

$$g(D) = 1 + D^{14} + D^{15} \quad (1)$$

where D is a single bit delay element. The polynomial forms not only a maximal length sequence, but also is a primitive polynomial. By the given generator polynomial, the corresponding pseudorandom number is generated as:

$$x_n = x_{n-14} \oplus x_{n-15}, \quad n = 0, 1, 2, \dots \quad (2)$$

where \oplus denotes modulo-2 addition. The following sequence defines the initialization sequence,

$$\mathbf{x}_{init} = [x_1 \ x_2 \ x_3 \ x_4 \ x_5 \ x_6 \ x_7 \ x_8 \ x_9 \ x_{10} \ x_{11} \ x_{12} \ x_{13} \ x_{14} \ x_{15}] \quad (3)$$

The scrambled data bits, s_n , are obtained as follows:

$$s_n = b_n \oplus x_n \quad (4)$$

where b_n represents the unscrambled data bits. The data stream de-scrambler at the receiver shall be initialized with the same initialization vector, \mathbf{x}_{init} , used in the transmitter scrambler. The initialization vector is determined from the seed identifier contained in the PHY header of the received packet. The seed identifier is included in the PHY header as detailed in 4.5.1.2.

The 15-bit seed value chosen shall correspond to the seed identifier, shown in

Table 4. The seed identifier value is set to 00 when the PHY is initialized and is incremented in a 2-bit rollover counter for each packet that is sent by the PHY. The value of the seed identifier that is used for the packet is sent in the PHY header.

The 15-bit seed value is configured as follows. At the beginning of each PHY frame, the register is cleared, the seed value is loaded, and the first scrambler bit is calculated. The first bit of data of the MAC header is modulo-2 added with the first scrambler bit, followed by the rest of the bits in the MAC header, frame body, and FCS.

Table 4 – Scrambler seed selection

SEEDID	Seed Value ($x-1, x-2 \dots x-15$)	Scrambler Output (first 16 bits) $x_0, x_1 \dots x_{15}$ (x_0 output first)
0	0011 1111 1111 111 ₂	0000 0000 0000 1000 ₂
1	0111 1111 1111 111 ₂	0000 0000 0000 0100 ₂
2	1011 1111 1111 111 ₂	0000 0000 0000 1110 ₂
3	1111 1111 1111 111 ₂	0000 0000 0000 0010 ₂

4.8 Forward error correction (FEC)

Depending on the mode of operation, scrambled data bits shall be encoded by the LDPC encoder of rate $r=1/2$. Rate $r=2/3$ encoding is achieved through puncturing as described later in this section.

LDPC Encoder is defined by the following parameters:

- K Data word length (un-coded block length)
- N Code word length (coded block length)
- $M = N - K$ Parity-check word length

For rate $r=1/2$, the following parameters are specified: $K=384$, $N=768$, and $M=384$.

The parity check matrix is composed of two sub-matrices,

$$\mathbf{H} = [\mathbf{H}^p \mid \mathbf{H}^d]$$

where \mathbf{H}^p is an $M \times M$ square matrix and \mathbf{H}^d is an $M \times K$ matrix.

The \mathbf{H}^p sub-matrix has a dual-diagonal pattern:

$$\mathbf{H}^p = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

The \mathbf{H}^d sub-matrix is given by:

$$H_{(\frac{1}{2})}^d = \begin{bmatrix} \pi_A & \pi_B & \pi_C & \pi_D \\ \pi_B & \pi_C & \pi_D & \pi_A \\ \pi_C & \pi_D & \pi_A & \pi_B \\ \pi_D & \pi_A & \pi_B & \pi_C \end{bmatrix}$$

where π_A , π_B , π_C , and π_D are permutation matrices of the identity matrix. π_B is a 90-degree rotation of π_A , and π_C is a 90-degree rotation of π_B and so on. Sub-matrix π_A is defined by a permutation vector of length $1 \times K/4$.

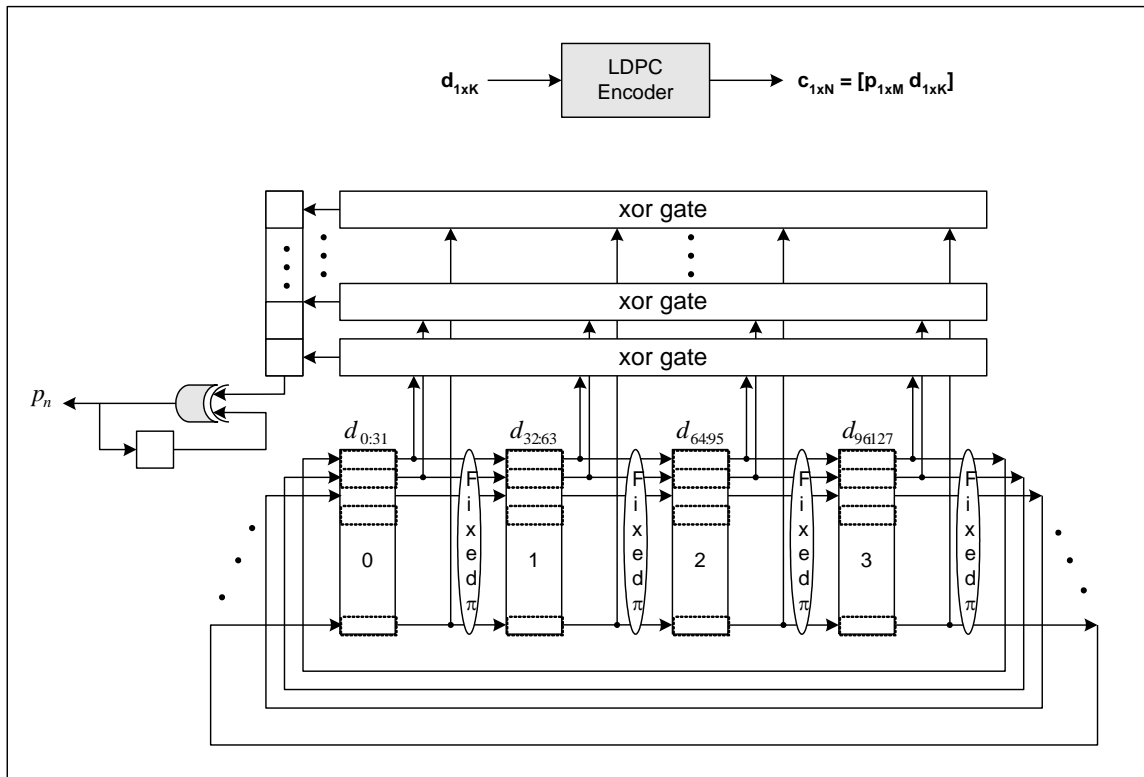


Figure 8 – LDPC encoder

The puncture pattern for the 2/3 rate shall follow a puncture pattern that is isolated ONLY to the parity bits where every other parity is punctured. The following steps outline the steps in the encoding of a 2/3 rate symbol from an encoded 1/2 rate symbol.

- a) Through the encoding process described for the 1/2 rate, encoded code-words, $C_{1x768} = [p_{1x384} d_{1x384}]$, are first generated
- b) Every other parity bit of p_{1x384} is punctured. The resultant pattern shall follow:

$$p_{1x384} = \{p_{1,1}, x, p_{1,3}, x, p_{1,5}, \dots, p_{1,383}, x\}$$

- c) This punctured p_{1x384} is then proceeded by p_{1x384} to result a 2/3 code word.

4.9 Data modulation

The C-UWB PHY layer supports data communication using BPSK/QPSK modulations. BPSK modulation (that is, polarity modulation) enables low-complexity architectures. Every compliant device will be able to both transmit and

receive BPSK modulated signals. In QPSK, the data mapping is identical to BPSK mapping, except that independent data streams are provided for each of the two orthogonal PHY channels.

4.10 Spreading and marker symbol insertion

Spreading codes provide for potentially multiple links within a single cable system. Marker Symbols are used to facilitate resynchronization and frequency/timing tracking at the receiver.

4.10.1 Spreading codes

For each cable link channel, there is a designated set of spreading codes for use with BPSK/QPSK. The first piconet uses the first spreading code listed in the table for the desired code length, and subsequent piconets use the next code sets in the order listed in the tables.

The first transmitted chip corresponds to the left most chip shown in the spread code tables.

Table 5 – G₂ spreading code sequences

Code Set	Orthogonal Code Sequence
	S_0S_1
1	++
2	+–

Table 6 – G₄ spreading code sequences

Code Set	Orthogonal Code Sequence
	$S_0 \dots S_3$
1	--+-
2	----+

3	+ - - -
4	+ - + +

Table 7 – G_8 spreading code sequences

Code Set	Orthogonal Code Sequence	
	$S_0 \dots S_3$	$S_4 \dots S_7$
1	+ + + -	- + - -
2	+ - + +	- + + +
3	+ - - +	+ + + +
4	+ - + +	- - - +
5	+ - - -	- + - -
6	+ - + +	+ - - -

Table 8 – G₆₄ spreading code sequences

Code Set	Orthogonal Code Sequence							
	$S_0 \dots S_3$	$S_4 \dots S_7$	$S_8 \dots S_{11}$	$S_{12} \dots S_{15}$	$S_{16} \dots S_{19}$	$S_{20} \dots S_{23}$	$S_{24} \dots S_{27}$	$S_{28} \dots S_{31}$
	$S_{32} \dots S_{35}$	$S_{36} \dots S_{39}$	$S_{40} \dots S_{43}$	$S_{44} \dots S_{47}$	$S_{48} \dots S_{51}$	$S_{52} \dots S_{55}$	$S_{56} \dots S_{59}$	$S_{60} \dots S_{63}$
1	-----	+----+	+--+--	---++	+++++	-+++-	-+++-	++--
	++--	-++-	-++-	++++	++--	-++-	-++-	++++
2	-+++	---++	+--+--	-----	-++-	-----	+---+	---++
	+--+	++--	-++-	++++	-++-	-----	+--+	---++
3	-+++	---++	+--+--	-----	-++-	-----	+---+	---++
	-+++	---++	+--+--	-----	+--+	++++	-+++	++--
4	-+++	++++	++--	-++-	+--+	-----	---++	+--+
	-++-	++--	++++	-+++	-++-	++--	++++	-++-
5	-----	+----+	+--+--	---++	-----	+--+	+--+	---++
	++--	-++-	-++-	++++	---++	+--+	+--+	-----
6	-+++	++++	++--	-++-	-+++	++++	++--	-++-
	-++-	++--	++++	-+++	+--+	---++	-----	+--+

Table 9 – G₁₂₈ spreading code sequences

Code Set	Orthogonal Code Sequence							
	$S_4 \dots S_7$	$S_8 \dots S_{11}$	$S_{12} \dots S_{15}$	$S_{16} \dots S_{19}$	$S_{20} \dots S_{23}$	$S_{24} \dots S_{27}$	$S_{28} \dots S_{31}$	
	$S_{36} \dots S_{39}$	$S_{40} \dots S_{43}$	$S_{44} \dots S_{47}$	$S_{48} \dots S_{51}$	$S_{52} \dots S_{55}$	$S_{56} \dots S_{59}$	$S_{60} \dots S_{63}$	
	$S_{68} \dots S_{71}$	$S_{72} \dots S_{75}$	$S_{76} \dots S_{79}$	$S_{80} \dots S_{83}$	$S_{84} \dots S_{87}$	$S_{88} \dots S_{91}$	$S_{92} \dots S_{95}$	
	$S_{100} \dots S_{103}$	$S_{104} \dots S_{107}$	$S_{108} \dots S_{111}$	$S_{112} \dots S_{115}$	$S_{116} \dots S_{119}$	$S_{120} \dots S_{123}$	$S_{124} \dots S_{127}$	
1	+ - + -	+ - + -	+ - + -	- + - +	+ - - +	- + + -	+ - - +	+ - - +
	+ + - -	+ + - -	+ + - -	- - + +	+ + + +	- - - -	+ + + +	+ + + +
	+ - + -	+ - + -	- + - +	+ - + -	+ - - +	- + + -	- + + -	- + + -
	+ + - -	+ + - -	- - + +	+ + - -	+ + + +	- - - -	- - - -	- - - -
2	+ + - -	+ + - -	+ + - -	- - + +	+ - - +	- + + -	+ - - +	+ - - +
	+ - + -	+ - + +	- + - +	- - + -	+ + + +	+ - - -	- + + +	+ + + +
	+ + + -	- + + -	- - - +	+ + + -	- + - -	+ - + +	- - + +	- - + +
	- + - +	- + - +	- - + -	+ + - +	- + + +	- - - -	- - - -	- - - -
3	+ + + -	+ - + +	+ + + -	- + - -	+ + - +	+ - - -	+ + - +	- + + +
	- - - +	- + - -	- - - +	+ - + +	+ + - +	+ - - -	+ + - +	- + + +
	+ + + -	+ - + +	- - - +	+ - + +	+ + - +	+ - - -	- - + -	+ - - -
	- - - +	- + - -	+ + + -	- + - -	+ + - +	+ - - -	- - + -	+ - - -
4	+ + - +	+ - - -	+ + - +	- + + +	+ + -	+ - - -	+ + - +	- + + +
	+ + - +	+ - - -	- - + -	+ - - -	- - + -	- + + +	+ + - +	- + + +
	+ + - +	+ - - -	+ + - +	- + + +	- - + -	- + + +	- - + -	+ - - -
	+ + - +	+ - - -	- - + -	+ - - -	+ + - +	+ - - -	- - + -	+ - - -
5	+ + + -	+ - + +	+ + + -	- + - -	- - + -	- + + +	- - + -	+ - - -
	+ + + -	+ - + +	- - - +	+ - + +	- - + -	- + + +	+ + - +	- + + +
	+ + + -	+ - + +	+ + + -	- + - -	- - + -	- + + +	- - + -	+ - - -
	- - - +	- + - -	+ + + -	- + - -	+ + - +	+ - - -	- - + -	+ - - -
6	+ + + -	+ + - +	+ + + -	- - + -	- - - +	- - + -	+ + + -	- - + -
	+ - + +	+ - - -	+ - + +	- + + +	- + - -	- + + +	+ - + +	- + + +
	+ + + -	+ + - +	+ + + -	- - + -	- - - +	- - + -	+ + + -	- - + -
	- + - -	- + + +	- + - -	+ - - -	+ - + +	+ - - -	- + - -	+ - - -

4.10.2 Marker symbol insertion

Marker Symbol, used to facilitate resynchronization and frequency/timing tracking at the receiver shall be transparently inserted and removed by the PHY every 24576 chips.

Marker Symbol consists of eight G_{128} (Golay code length 128 length) block preceded and proceeded by 64 chip prefix and postfix. Prefix codes are defined to include the first 64 chips of the same Golay block G_{128} , and postfix codes are cyclic extensions of the same Golay block G_{128} . Hence the extended symbol is defined as:

$$GE = \text{Prefix } G_{128} + (8 \times G_{128}) + \text{Postfix } G_{128} = 1152 \text{ chips}$$

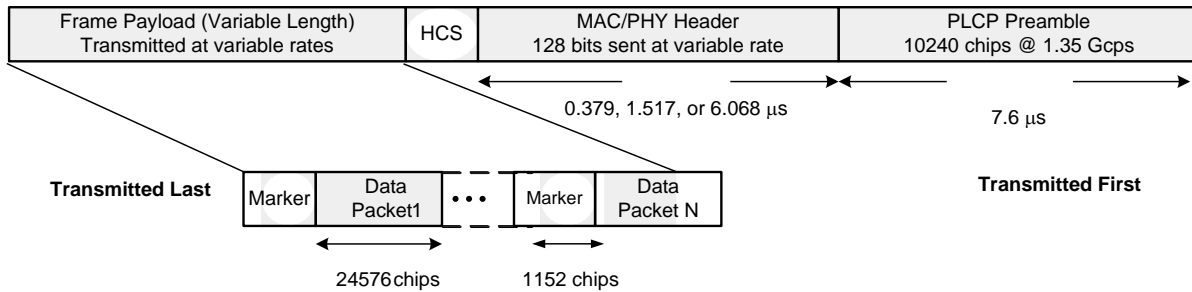


Figure 9 – Marker symbol insertion

4.11 Operations

The 3 dB bandwidth of the baseband signal is specified to occupy 1.35 GHz.

4.11.1 Regulatory compliance

The regulatory documents defining the maximum allowable radiated power spectral density, as specified by the appropriate regulatory bodies, are shown in Table. The radiated/unintentional emissions in the US are subject to FCC Part 15 regulations for unintentional emissions. The EU directive for CE compliance on electromagnetic compatibility is “89/336/EEC”. In addition, compliance with the low voltage equipment directive 73/23/EEC is necessary. The title of the relevant standard is EN 61000-6-1:2001 Electromagnetic compatibility (EMC) Part 6-1: Generic standards – Immunity for residential, commercial and light-industry environments. The reference number for this standard is IEC 61000-6-1.

Table 10 – Maximum emission levels

Geographical Region	Regulatory Document
Europe	IEC 61000-6-1
USA	47 CFR 15 sub-parts A, B, and C See informational Annex B

4.11.2 Operating temperature range

A conformant implementation shall meet all of the specifications in this standard for ambient temperatures from 0 to 40°C.

4.12 Transmitter

The transmitter is specified in terms of its output signal characteristics.

4.12.1 Baseband signal

The base-band reference pulse has nominal chip duration T_{chip} of 740.74 ps. The base-band reference pulse spectrum for the complete transmitter and receiver system is a root raised cosine low pass filter with 30% excess bandwidth ($\beta=0.3$),

$$S(f) = \begin{cases} T_{chip} & \text{for } 0 \leq |f| \leq \frac{1-\beta}{2T_{chip}} \\ \frac{T_{chip}}{2} \left\{ 1 + \cos \left[\frac{\pi T_{chip}}{\beta} \left(|f| - \frac{1-\beta}{2T_{chip}} \right) \right] \right\} & \text{for } \frac{1-\beta}{2T_{chip}} \leq |f| \leq \frac{1+\beta}{2T_{chip}} \\ 0 & \text{for } |f| \geq \frac{1+\beta}{2T_{chip}} \end{cases}$$

The transmitter pulse spectrum is the square root of this spectrum and may be defined in the time domain as the impulse response of the root raised cosine filter, the square root of the filter spectrum described above, and is

$$r(t) = \frac{4\beta}{\pi\sqrt{T_{chip}}} \frac{\cos\left(\frac{\pi t(1+\beta)}{T_{chip}}\right) + \frac{T_{chip}}{4\beta t} \sin\left(\frac{\pi t(1-\beta)}{T_{chip}}\right)}{\left(1 - \left(\frac{4t\beta}{T_{chip}}\right)^2\right)}$$

The reference pulse is translated to the operating frequency by $\cos(2\pi ft)$ and by $\sin(2\pi ft)$ to obtain two essentially orthogonal pulses $r_I(t)$ and $r_Q(t)$. Either of the pulses can be polarity modulated in a fashion analogous to BPSK in conventional radio. Both pulses $r_I(t)$ and $r_Q(t)$ can each be independently polarity modulated with the signals added together to form a 4-level encoding scheme analogous to QPSK in conventional radio.

The transmitted pulse shape $p_{TX}(t)$ should be constrained by the shape of its cross correlation function with a standard reference pulse $r(t)$. For the purposes of testing a transmitter pulse for compliance we define the cross correlation $X(\tau)$ of the transmitter pulse $p_{TX}(t)$ with $r(t)$ as

$$X(\tau) = \frac{1}{\sqrt{P_{TX}R}} \int_{-\infty}^{\infty} r(t)p_{TX}(t+\tau)dt$$

where P_{TX} is the energy in the transmitter pulse $p_{TX}(t)$, and R is the energy in the reference pulse $r(t)$. The cross correlation $X(\tau)$ for a compliant transmitter is greater than 0.707 for a continuous range of τ surrounding the peak cross correlation value, and the range of τ shall be equal to a width of at least 0.2 ns. In addition, the remaining side-lobes of the correlation function should be less than or equal to 0.3. While the measurement described here occurs on the pulse envelope as if shaping is done at base-band, it is not the intention of the standard to imply that pulse shaping shall occur only at base-band.

The base-band referred transmitted impulse response shall have a normalized peak cross-correlation within 3 dB of this reference pulse. For BPSK this base band pulse is polarity modulated and shifted to the operating center frequency f_c by $\cos(2\pi f_c t)$. For QPSK a polarity modulated orthogonal signal is generated by shifting with $\sin(2\pi f_c t)$.

4.12.2 Transmit Power Spectrum Density (PSD) mask

The transmitted signal PSD shall comply with section 4.11.1. The out-of-band PSD should remain below the PSD given by Figure 11.

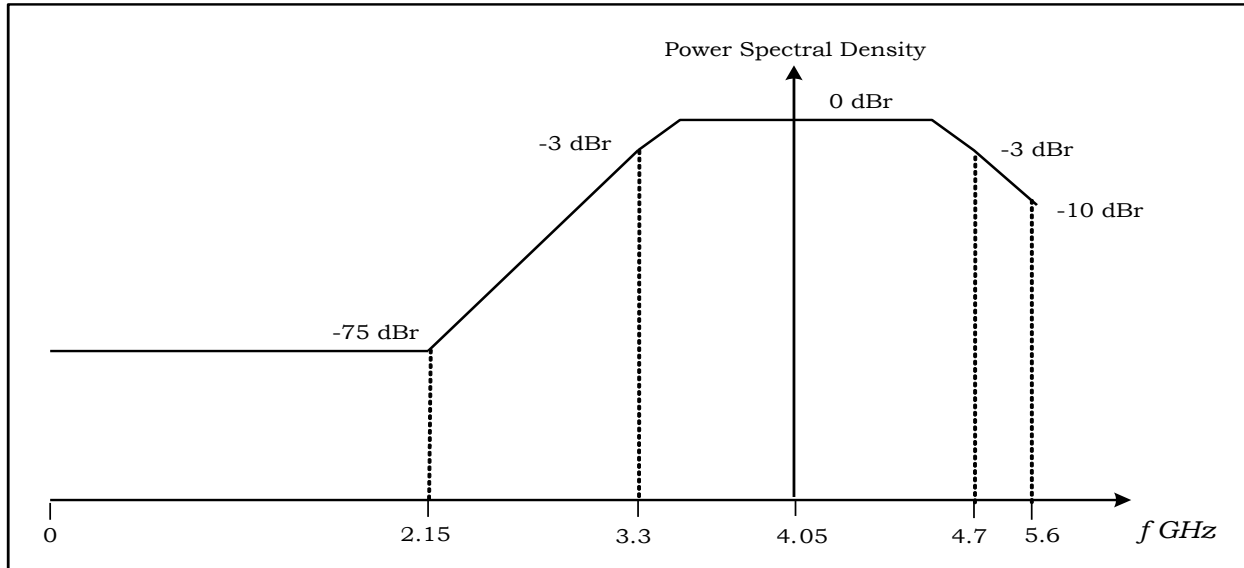


Figure 10 – Transmit PSD mask

4.12.3 Transmit power control

Subject to regulation limits given in section 4.11.1, the transmitter shall be adjustable to allow operations up to 30 dB below the maximum allowable PSD.

4.12.4 Chip rate clock and chip center frequency alignment

The transmitted center frequency and chip clock frequency tolerances shall be ± 10 ppm maximum.

4.13 Receiver

The receiver performance is specified in terms of the average power expressed in dBm (decibels relative to one milliwatt) contained in the UWB bandwidth.

4.13.1 Receiver sensitivity

For a packet error rate (PER) of less than 1% with a PSDU of 1024 bytes, the minimum receiver sensitivity numbers for the various rates and modes are listed in Table 11.

Table 11 – Receiver performance requirements

Data Rate (Mb/s)	Minimum Sensitivity (dBm)
21	-84
84	-78
169	-76
338	-73

675	-70
1350	-67
2700	-64

4.13.2 Receiver CCA performance

The start of a valid transmission at a receiver level equal to or greater than the minimum sensitivity shall cause CCA to indicate busy with a probability >90% within 5 microseconds. If the preamble portion was missed, the receiver shall hold the carrier sense (CS) signal busy for any signal 20 dB above the minimum sensitivity.

4.13.3 Receiver maximum input level

The receiver maximum input level is the maximum power level of the incoming signal, in dBm, present at the input of the receiver for which the error rate criterion is met. A compliant receiver shall respond correctly at a maximum input level of at least -25 dBm for each of the modulation formats that the device supports.

4.14 Timing

The values for the C-UWB PHY layer timing parameters are defined in Table 12.

Table 12 – C-UWB PHY layer timing parameters

PHY Parameter	Value (μ s)
<i>pPHYMIFSTime</i>	0
<i>pPHYSIFSTime</i>	5
<i>pCCADetectTime</i>	5
<i>pPHYChannelSwitchTime</i>	100

4.14.1 Inter-frame spacing

The inter-frame spacing parameters are given in Table 13.

Table 13 – Inter-frame spacing parameters

802.15.3 MAC Parameter	Corresponding PHY Parameter
<i>MIFS</i>	<i>pPHYMIFSTime</i>
<i>SIFS</i>	<i>pPHYSIFSTime</i>
<i>pBackoffSlot</i>	<i>pPHYSIFSTime</i> + <i>pCCADetectTime</i>
<i>BIFS</i>	<i>pPHYSIFSTime</i> + <i>pCCADetectTime</i>
<i>RIFS</i>	2 x <i>pPHYSIFSTime</i> + <i>pCCADetectTime</i>

4.14.2 Receive-to-transmit turnaround time

The RX-to-TX turnaround time shall be less than *pPHYSIFSTime*. The RX-to-TX turnaround time shall be measured at the coax interface from the trailing edge of the last symbol received until the first symbol of the PHY preamble is present at the coax interface.

4.14.3 Transmit-to-receive turnaround time

The TX-to-RX turnaround time shall be less than $pPHYSIFSTime$. The TX-to-RX turnaround time shall be measured at the coax interface from the trailing edge of the last transmitted symbol until the receiver is ready to begin the reception of the next PHY packet.

4.14.4 Time between successive transmissions

The time between successive transmissions shall be $pPHYMIFSTime$ and measured at the coax interface from the trailing edge of the last symbol transmitted until the first symbol of the PHY preamble is present at the coax interface.

4.14.5 Channel switch time

The channel switch time is defined as the time from when the last valid bit is received at the coax interface on one Channel Time Allocation (CTA) until the DEV is ready to transmit or receive on a new Channel Time Allocation (CTA). The channel switch time shall be less than $pPHYChannelSwitchTime$.

4.15 Management

The C-UWB PHY PIB (Piconet Information Base) comprises the managed objects, attributes and notifications required to manage the PHY layer of a DEV.

Table 14 – C-UWB PHY PIB definition

Bits	Content	Description
b0-b19	Supported Data Rates	20-bit field that indicates supported data rates indicated in DATA field. Reference: Table 1. If a combination of n DATA rates is supported, the field shall be set to 1 at the n-th bit. For example, if DATA rates 1,3,5, and 20 are selected, this field shall be encoded to include: [10101000000000000001]
b20-b21	FEC Type	2 bit field that indicates supported FEC types 00 = no FEC 01 = LDPC rate 1/2 10 = LDPC rate 2/3 11 = Reserved for future use
b22-b24	Spreading Codes	3 bit field that indicates supported spreading lengths 000 = spreading length 64 only 001 = spreading lengths 64 and 8 010 = spreading lengths 64, 8 and 4 011 = spreading lengths 64, 8, 4, and 2 100 = spreading lengths 64, 8, 4, 2, and 1 101, 111 = Reserved for future use
b25	Modulation	1 bit field that indicates supported modulation types 0 = BPSK 1 = QPSK
b26-b27	Header Type	2 bit field that indicates header spreading length 00= spreading length 64 (Default) 01= spreading length 16 10= spreading length 4 00= Reserved
b28- b31	Reserved	5 bit field that indicates support for future use.

4.15.1 Fragment size encoding

The encoding of the preferred fragment size used in the Capability IE is given in Table 15.

Table 15 – C-UWB PHY preferred fragment size encoding

Value	Preferred Fragment Size (octets)
0	<i>pMaxFrameBodySize</i>
1	12096
2	8064
3	6048
4	4032
5	2016
6	1008
7	<i>pMinFragmentSize</i>

The PHY definitions create restrictions on the maximum frame size, maximum transfer unit size and minimum fragmentation size that will be supported. These parameters are defined in this clause.

4.15.2 Maximum frame length

The maximum frame length allowed, *pMaxFrameBodySize*, shall be 16232 octets. This total includes the frame body and FCS but not the PHY preamble, PHY header or MAC header.

4.15.3 Minimum and maximum transfer unit size

The maximum size data frame passed from the upper layers, *pMaxTransferUnitSize*, shall be 16232 octets. If security is enabled for the data connection, the upper layers should limit data frames to 16232 octets minus the security overhead.

The minimum size data frame passed from the upper layers, *pMinTransferUnitSize*, shall be 1500 octets. If security is enabled for the data connection, the upper layers should limit data frames to 1500 octets minus the security overhead.

4.15.4 Minimum fragment size

The minimum fragment size, *pMinFragmentSize*, shall be 504 octets.

Annex A (Informative)

Summary of emission limits

Table A-1 shows a representation of the maximum permissible emissions for the USA. The radiated/unintentional emissions in the USA are subject to FCC Part 15 regulations for unintentional emissions, and the latest Part 15 regulations apply. As a guide, the measurement standards and requirements are summarized below.

Table A-1 – FCC Part 15 Unintentional emission limits

Frequency (F) (MHz)	Detector Resolution (kHz)	Field Strength ($\mu\text{V/m}$)	Measurement Distance (m)
$0.009 < F \leq 0.15$	0.2	$2400 / F$	300
$0.15 < F \leq 0.49$	9	$2400 / F$	300
$0.49 < F \leq 1.705$	9	$24000 / F$	30
$1.705 < F \leq 30$	9	30	30
$30 < F \leq 88$	120	100	3
$88 < F \leq 216$	120	150	3
$216 < F \leq 960$	120	200	3
$960 < F \leq 1000$	120	500	3
$F > 1000$	1000	500	3

In the emission table above, the tighter limit applies at the band edges. The emission limits shown in the above table are based on measurements employing a CISPR quasi-peak detector except for the frequency bands 9-90 kHz, 110-490 kHz and above 1000 MHz. Radiated emission limits in these three bands are based on measurements employing an average detector. The Unintentional Emission limits of Part 15.109 apply, including paragraph (e) which references Section 15.209 “Radiated emission limits, general requirements” for frequencies below 30 MHz. CISPR Publications 16 defines the CISPR Quasi –peak detector. Note that the detector bandwidth varies with frequency.

Intentional and unintentional radiators are to be measured for compliance using the following procedure excluding sections 4.1.5.2, 5.7, 9 and 14: ANSI C63.4–2003: “Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electronic Equipment in the Range of 9 kHz to 40 GHz” (incorporated by reference, see § 15.38).

Annex B (Normative)

Compliance

This annex is intended to assist designers, implementers and conformance test developers; it provides a concise summary of mandatory and optional features and, for each feature, reference to the governing normative clauses.

A device that conforms to this specification shall implement all mandatory C-UWB PHY layer functions and may implement any optional PHY layer functions summarized by Table B-1. Providers of devices that claim conformance to this technical specification are encouraged to complete a similarly organized Protocol Implementation Conformance Statement (PICS), whose purpose is to provide a quick reference to the PHY capabilities and options implemented.

Table B-1 – C-UWB PHY Conformance Requirements

Item Number	Item Description	Reference	Status
PLF 1	PPDU frame format	6.3	M
PLF 1.1	PPDU encoding	6.3.1	M
PLF 1.2	PPDU Rate Dependent Parameters	6.3.2 Table- 2	M
PLF 1.3	PPDU timing parameters	6.3.3	M
PLF 2	PPDU preamble	6.4	M
PLF 2.1	PPDU synchronization (SYNC) field	6.4.1	M
PLF 2.2	PPDU start frame delimiter (SFD) field	6.4.2	M
PLF 3	Frame header	6.5	M
PLF 3.1	PHY header	6.5.1	M
PLF 4	Forward Error Correction (FEC), Rate 1/2	6.8	M
PLF 4.1	Forward Error Correction (FEC), Rate 2/3	6.8	O
PLF 5	Data Modulation	6.9	
PLF 5.1	BPSK	6.9	M
PLF 5.2	QPSK	6.9	O

Item Number	Item Description	Reference	Status
PLF 6	Spreading and marker symbol insertion	6.10	M
PLF 6.1	Spreading codes	6.10.1	M
PLF 6.2	Marker symbol insertion	6.10.2	M
PLF 7	Operations	6.11	M
PLF 7.1	Regulatory compliance	6.11.1	M
PLF 7.2	Operating temperature range	6.11.2	M
PLF 7.3	Transmit PSD mask	6.12.2	M
PLF 7.4	Transmit power control	6.12.3	M
PLF 7.5	Chip rate clock and chip center frequency alignment	6.12.4	M
PLF 7.6	Receiver sensitivity	6.13.1	M
PLF 7.7	Receiver CCA performance	6.13.2	M
PLF 7.8	Receiver maximum input level	6.13.3	M
PLF 8	Timing	6.14	M
PLF 9	Maximum frame length	6.15.2	M
PLF 9.1	Minimum and maximum transfer unit size	6.15.3	M
PLF 9.2	Minimum fragment size	6.15.4	M