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Power Specification Part 3: Power Distribution Management

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Abstract:
This specification defines an architecture for the management of power distributed within power domains (i.e. power source to a power sink on the 1394 serial bus).

Keywords:
1394, Power, Source, Sink, Distribution, Management, Legacy, PDM, DEP, Message Packet, node power manager.

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1. Overview

IEEE Std 1394-1995, Standard for a High Performance Serial Bus, and its supplements, IEEE 1394a-2000 and IEEE P1394b, provide for definitions in the 1394 cable environment for the distribution of power to connected devices. Although rudimentary facilities are specified to permit Serial Bus devices to report their power requirements (*i.e.*, the *pwr_class* field in the self ID packets), the standard does not provide sufficient definition of power distribution management that would enable different vendors to implement power distribution management protocols that guarantee interoperability of devices on the bus.

This specification will provide the definitions that, when followed, will provide a level of interoperability between devices on the bus that expect to provide power to the bus and devices on the bus that expect to be able to sink power from the bus.

1.1 Purpose

This specification clarifies (and in some instances, extend) the power distribution management facilities of IEEE Std 1394-1995 and its amendments IEEE1394a-2000 and IEEE P1394b, to achieve the following goals:

- Enable standard power distribution management to Serial Bus powered devices for the purpose of promoting integration into computer systems or other peer devices (i.e. set top boxes, or any other device delivering power to the serial bus);
- Enable an orderly method by which Serial Bus powered devices may be given a link-on within the bounds of available power in their power domain;
- Provide a transaction layer protocol by which an application may increase the power efficiency of a Serial Bus it is associated with by enabling it to control the energy consumption levels of the device.
- Improve the perception of device availability through better power distribution management techniques that provide the capability of notifying the user which device is not able to be cable-powered and which are enabled to be cable-powered.

1.2 Scope

This specification is about the manipulation of 1394-bus specific power control mechanisms by software entities residing on the bus for the purpose of conserving power while maximizing device availability for end-users. While any entity on the Serial Bus may provide the described control, the intention is that software running on an intelligent computing device (such as a personal computer) would best implement Serial Bus-wide power distribution management.

The software that provides power distribution management control for units within all the managed nodes on the Serial Bus is called the Power Distribution Manager (PDM). There is only one PDM on the Serial Bus at any one moment in time. Not all nodes on the Serial Bus are managed by PDM. Only cable-powered devices on the serial bus shall be managed by PDM.

Additionally, PDM only manages the bus interface (i.e. the PHY and the Link). Power consumption management of the units and sub-units within a node are the responsibility of the node manager (a feature/function internal to the node firmware/software).

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2. References

The following standards contain provisions that, through reference in this document, constitute provisions of this specification. All the standards listed are normative references. Informative references are given in appropriate Annexes of this specification. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this specification are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below.

[R1] IEEE Std 1394-1995, Standard for a High Performance Serial Bus and its amendments: IEEE 1394a-2000 and IEEE P1394b

[R2] IEEE P1212

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3. Definitions

3.1 Conformance Levels

3.1.1 expected: A key word used to describe the behavior of the hardware or software in the design models *assumed* by this Specification. Other hardware and software design models may also be implemented.

3.1.2 may: A key word that indicates flexibility of choice with *no implied preference*.

3.1.3 shall: A key word indicating a mandatory requirement. Designers are *required* to implement all such mandatory requirements.

3.1.4 should: A key word indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase *is recommended*.

3.1.5 reserved codes: A set of codes for a reserved field that are defined in this specification, but not otherwise used. Future specifications may implement the use of these codes. A product implementing this specification shall not generate, nor receive these codes.

3.1.6 reserved fields: A set of bits for a reserved field that are defined in this specification, but are not otherwise used. Products that implement this specification shall zero these fields and shall not check the reserved field's value. Products that implement future revisions of this specification may set these codes as defined by the specification.

3.2 Glossary of Terms

3.2.1 byte: Eight bits of data, used as a synonym for octet.

3.2.2 CSR Architecture: A convenient abbreviation of the following reference (see clause 2): IEEE P1212, Information Technology—Microprocessor systems— Control and Status Register (CSR) Architecture for Microcomputer Buses.

3.2.3 doublet: Two bytes, or 16 bits, of data

3.2.4 initial node space: The 256 terabytes of Serial Bus address space that is available to each node. Addresses within initial node space are 48 bits and are based at zero. The initial node space includes initial memory space, private space, initial register space and initial units space. See IEEE P1212 and IEEE Std 1394-1995 for more information on address spaces.

3.2.5 initial register space: A one kilobyte portion of initial node space with a base address of FFFF F000 0000_{16}. Core registers defined by ISO/IEC 13213:1994 are located within initial register space as are Serial Bus-dependent registers defined by IEEE Std 1394-1995.

3.2.6 initial units space: A portion of initial node space with a base address of FFFF F000 0400_{16}. This places initial units space adjacent to and above initial register space. The CSRs and other facilities defined by unit architectures are expected to lie within this space.

3.2.7 kilobyte: A quantity of data equal to 2^{10} bytes.

3.2.8 Legacy: Characteristics or behavior of a link, node, PHY, cable or connector defined by IEEE Std 1394-1995 or IEEE Std 1394a-2000.

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3.2.9 node ID: The 16-bit node identifier defined by IEEE Std 1394-1995 that is composed of a bus ID portion and a physical ID portion. The physical ID is uniquely assigned as a consequence of Serial Bus initialization.

3.2.10 node power manager: a firmware/software component of a node that manages the energy consumption and power states of the units and sub-units integral to the node.

3.2.11 octlet: Eight bytes, or 64 bits, of data.

3.2.12 OUI: Organizationally Unique Identifier

3.2.13 power domain: A portion of the Serial Bus topology that receives power from a single power source. The fact that cable power shall not be propagated by nodes that supply power, along with other power class and topology information in the self ID packets, permits the power manager to parse a Serial Bus topology into disjoint power domains.

3.2.14 quadlet: Four bytes, or 32 bits, of data.

3.2.15 register: A term used to describe quadlet aligned addresses that may be read or written by Serial Bus transactions. In the context of this specification, the use of the term register does not imply a specific hardware implementation. For example, in the case of split transactions that permit sufficient time between the request and response subactions, the behavior of the register may be emulated by a processor within the module.

3.2.16 split transaction: A transaction that consists of separate request and response subactions. Subactions are considered separate if ownership of the bus is relinquished between the two. A transaction that is not split is called a unified transaction.

3.2.17 terabyte: A quantity of data equal to 2^{40} bytes.

3.2.18 transaction: An exchange between a requester and a responder that consists of a request and a response subaction. The request subaction transmits a Serial Bus transaction such as quadlet read, block write or lock, from the requesting node to the node intended to respond. Some Serial Bus commands include data as well as transaction codes. The response subaction returns completion status and sometimes data from the responding node to the requesting node.

3.2.19 unified transaction: A transaction in which the request and response subactions are completed as an indivisible sequence. Between the initiation of the request and the completion of the response, subactions by nodes other than the requester or the responder are blocked. A transaction that is not unified is called a split transaction.

3.2.20 unit: A component of a Serial Bus node that provides processing, memory, I/O or some other functionality. Once the node is initialized, the unit provides a CSR interface that is typically accessed by device driver software at an initiator. A node may have multiple units, which normally operate independently of each other.

3.2.21 unit architecture: The specification of the interface to and the behaviors of a unit implemented within a Serial Bus node.

3.3 Acronyms and Abbreviations

The following are abbreviations and or acronyms that are used in this specification:

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CRC	Cyclical redundancy checksum
EUI-64	Extended Unique-Identifier, 64-bit
DEP	Discovery and Enumeration Protocol
PDM	Power Distribution Manager
PDMS	Power Distribution Management Specification
BM	1394 Bus Manager
LLO	Legacy Link Off message request packet

3.4 Notation

The following conventions should be understood by the reader in order to comprehend this specification.

Decimal, hexadecimal, and occasionally, binary numbers are used within this specification. By editorial convention, decimal numbers are most frequently used to represent quantities or counts. Addresses are uniformly represented by hexadecimal numbers. Hexadecimal numbers are also used when the value represented has an underlying structure that is more apparent in a hexadecimal format than in a decimal format. Binary numbers are used infrequently and generally limited to the representation of bit patterns within a field.

Decimal numbers are represented by Arabic numerals without subscripts or by their English names. Hexadecimal numbers are represented by digits from the character set 0 – 9 and A – F followed by the subscript 16. Binary numbers are represented by digits from the character set 0 and 1 followed by the subscript 2. For the sake of legibility, binary and hexadecimal numbers are separated into groups of four digits separated by spaces.

As an example, 42, $2A_{16}$ and $0010\ 1010_2$ all represent the same numeric value.

3.4.1 Bit, byte and quadlet ordering

This specification uses and extends the facilities of Serial Bus, IEEE Std 1394-1995, and therefore uses the ordering conventions of Serial Bus in the representation of data structures. In order to promote interoperability with memory buses that may have different ordering conventions, this specification defines the order and significance of bits within bytes, bytes within quadlets and quadlets within octlets in terms of their relative position and not their physically addressed position.

Within a byte, the most significant bit, msb, is that which is transmitted first and the least significant bit, lsb, is that which is transmitted last on Serial Bus, as illustrated below. The significance of the interior bits uniformly decreases in progression from msb to lsb.

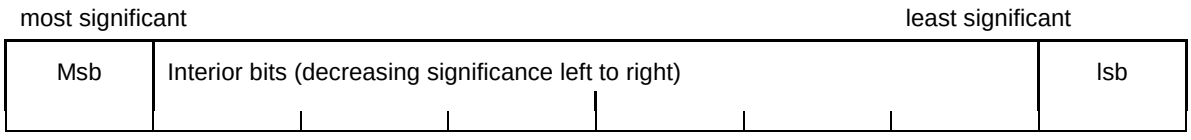

Figure 3-1 Bit ordering within a byte

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Within a quadlet, the most significant byte is that which is transmitted first and the least significant byte is that which is transmitted last on Serial Bus, as shown below.

most significant least significant

most significant byte			least significant byte

Figure 3-2 Byte ordering within a quadlet

Within an octlet, which is frequently used to contain 64-bit Serial Bus addresses, the most significant quadlet is that which is transmitted first and the least significant quadlet is that which is transmitted last on Serial Bus, as the figure below indicate.

most significant

most significant quadlet
least significant quadlet

least significant

Figure 3-3 Quadlet ordering within an octlet

Increasing Serial Bus addresses for quadlets correspond to increasing addresses on other buses bridged to Serial Bus, but the correlation of addresses is problematical when block transfers take place that are not quadlet aligned or not an integral number of quadlets. In such cases, no assumptions may be made about the ordering (significance within a quadlet) of bytes at the unaligned beginning or fractional quadlet end of such a block transfer, unless an application has knowledge (outside of the scope of this specification) of the ordering conventions of the other bus.

3.4.2 Register specifications

This specification precisely defines the format and function of control and status registers, CSRs. Some of these registers are read-only, some can be both read and written and some generate special side effects subsequent to a write. In order to precisely define CSRs, their bit fields, their initial values and the effects of read, write or other transactions, the format illustrated in the figure below is used.

definition

most significant least significant

bus-dependent	reserved	unit-dependent	vendor-dependent	cmnd	flag

initial value

$3F_{16}$	zero	unit-dependent	42	zero

read value

last write	zero	last write	last update	cmnd	flag

write effects

stored	Ignored	stored	ignored	w	u

Figure 3-4 CSR specification example

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The register definition contains the names of register fields. The names are intended to be descriptive, but the fields are defined in the text; their function should not be inferred solely from their names. However, the following register definition field names have defined meanings. Register field names are identified with a unique font: `example of a field name font`.

Table 3-1 Example of register definition field names

Name	Abbreviation	Definition
`bus-dependent`	`bus-depend`	The meaning of the field shall by defined by the bus specification, in this case IEEE Std 1394-1995
`Reserved`	`R`	The field is reserved for future definition (see definitions)
`unit-dependent`	`unit-depend`	The meaning of the field shall be defined by the company or organization responsible for the unit architecture
`vendor-dependent`	`vendor-dependor`	The meaning of the field shall be defined by the node's vendor

CSRs shall assume initial values upon the restoration of power (a power reset) or upon a write to the node's RESET_START register (a command reset). If the power reset values differ from the command reset values, they shall be separately and explicitly defined. Initial values for register fields may be described as numeric constants or with one of the terms defined for the register definition. Values for register fields subsequent to a reset may be described in the same terms or as defined below.

Table 3-2 Register field values subsequent to a reset

Name	Abbreviation	Definition
unchanged	X	The field retains whatever value it had just prior to the power reset, bus reset or command reset.

In addition to numeric values for constant fields, the read values returned in response to a quadlet read transaction may be specified by the terms below.

Table 3-3 Read values returned in response

Name	Abbreviation	Definition
last write	W	The value of the field shall be either the initial value or, if a write or lock transaction addressed to the register has successfully completed, the value most recently stored in the field.[1]
last update	U	The value of the field shall be that most recently updated by the node hardware or software. An updated field value may be the result of a write effect to the same register address, a different register address or some other change of condition within the node.

[1] For clarity, read values for a field in a register that accepts lock transactions may be described as *last successful lock* rather than *last write*. However, the abbreviation in both cases remains *w*. Similar liberties may be taken with the use of *conditionally stored* in place of *stored* when the action occurs as the result of a lock transaction, but the corresponding one-letter abbreviation, *s*, is also unchanged.

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The effects of data written to the register shall be specified by the terms below.

Table 3-4 Effects of write data to a register

Name	Abbreviation	Definition
Effect	E	The value of the data written to the field may have an effect on the node's state, but the effect may not be immediately visible by a read of the same register. The effect may be visible in another register or may not be visible at all.
Ignored	I	The value of the data written to the field shall be ignored; it shall have no effect on the node's state.
Stored	S	The value of the data written to the field shall be immediately visible by a read of the same register; it may also have other effects on the node's state.

Reserved fields within a register shall be explicitly described with respect to initial values, read values and write effects. Initial values and read values shall be zero while write effects shall be ignored. CSRs that are not implemented, either because they are optional or they fall within a reserved address space, shall abide by these same conventions if a successful completion response is returned for a read, write or lock transaction.

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4. Power Distribution

Power distribution management and the Power Distribution Manager (PDM), specifically, enables power to as many cable-powered devices as possible. The PDM builds a knowledgebase of the capabilities of power providers in each power domain. The PDM tracks the power class information in the self-ID packet of serial bus power consumers (or potential consumers). The PDM uses the information it gathers in an attempt to prevent potential serial bus failures resulting from inappropriate use of cable power.

Message request/response packets are used by the PDM to perform the tasks associated with distributing and allocating power to serial bus power consumers, tracking power available from power providers, and determining when it is appropriate to send a link-on PHY configuration packet to power consumers that have had their links turned off. These same mechanisms are used when power consumers turn their link off, that is, their link ceases consuming cable power and have either their power allocation retained or returned to the pool of available power in the power domain. Message packets are also used by the PDM to determine when a node is ready to transact and respond to transactions on the serial bus.

Node feature and function discovery, i.e. the process of enumerating a node and its units, are key elements to the PDM, however, a detailed coverage of discovery and enumeration protocol (*DEP*) is beyond the scope of this specification. Details on DEP can be obtained from IEEE P1394.1 Annex C, “Discovery and Enumeration Protocol”.

4.1 Power distribution management Model

A PDMS compliant node shall have a Node_Power_Directory entry in the root directory of its configuration ROM. The Node_Power_Directory entry consists of the following entries:

- Extended Key Specifier ID,
- Extended Key,
- Node Power Leaf.

A PDMS compliant cable-powered node shall contain a Node PDM Registers entry in the Node Power Directory.

A node that does not contain a Node_Power_Directory entry in its root directory shall be managed as a *Legacy* node.

A power domain is a region of the serial bus whose cable power is provided by a single power provider.

The process of managing available power in a power domain takes place:

- When the PDM capable node has been successful in establishing itself as bus manager,
- When PDMS compliant device nodes (non-Legacy) become connected or disconnected from serial bus.
- When device nodes power requirements and/or status change

The PDM, executing as a feature/function of serial bus manager, directs the allocation and deallocation of power consumption among power consumers in a power domain. Applications utilize the features of power distribution management through the use of abstract application interfaces (message request/response transactions) that work with any device, regardless of its bus interface.

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Power distribution management is the process of computing the amount of power available within a 1394 bus power domain and transmitting a link-on PHY configuration packet to as many cable powered devices in that domain as possible. The PDM will, in turn, enable each cable-powered device in the power domain - facilitating discovery enumeration of that device. After a device node has been accessed for discovery enumeration, the PDM will send a link-off message to the node. Other device nodes will, in turn, go through the same process. When completed the PDM will have a topology map of all cable bus powered devices.

As applications are loaded, a search for an associated device takes place via DEP. When the desired device is found, the PDM will work in conjunction with DEP (in the instance of a cable-powered device) to enable power to that device (i.e. transmit a link-on PHY configuration packet and perform all processes required to bring the device to an active state). Message request/response packets are used to facilitate this process.

There may be instances where a power consumer exists in multiple power domains. The figure below is one embodiment of such an instance.

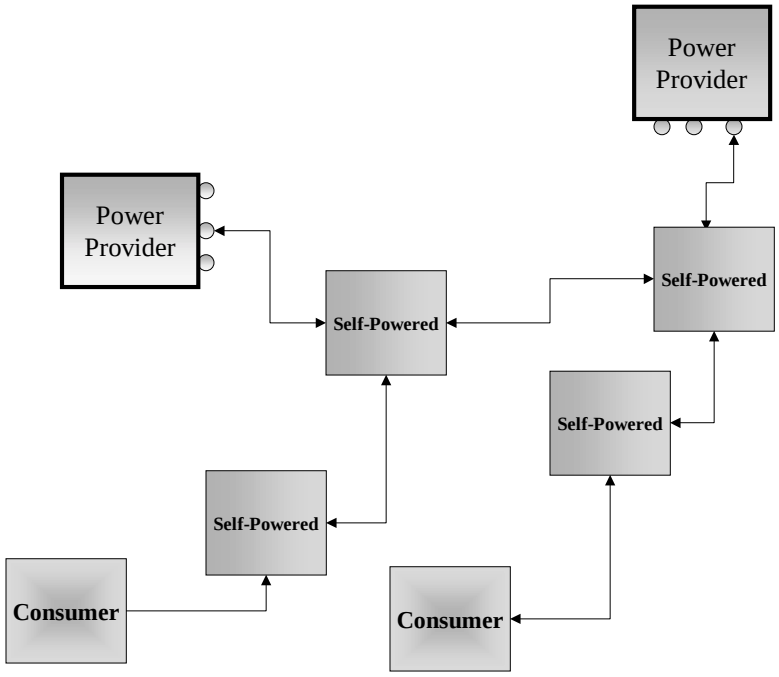

Figure 4-1 Power Consumers in a Multiple Power Domain

When configurations such as shown in the preceding figure exist, the PDM is not able to determine which power provider the power consumer derives its power. In these circumstances, the PDM shall deallocate from each power provider the amount of power required by all power consumers that could be consuming power from any power provider in the domain.

4.1.1 Power Policy and Policy Owners

Power policy, that is, the policy that establishes when devices (once they have been enumerated by the PDM and DEP) are powered on (i.e. sent a link-on PHY configuration packet) or powered off (i.e. link off message request is sent) and/or the policy that changes the power state of the interface to a node (i.e. the port) or the power state of a unit in a node is beyond the scope of this specification.

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4.1.2 Power Control

Within the IEEE 1394 standard, the PHY in any node may, when connected to serial bus, consume up to 3 watts of serial bus power. When determining the amount of power available in a power domain, power distribution management begins with an assumption that each node on the bus is consuming 3 watts. This establishes a baseline value for the amount of power available in the domain and whether the PDM will begin to transmit a PHY configuration packet to begin the node enumeration process.

The PDM may read the configuration status ROM of a node to determine it the PHY in the node consumes serial bus cable power or not.

The PDM enables a cable-powered node by sending the node a link-on PHY configuration packet. Once the node link has been enabled, the PDM is able to determine the precise amount of power the node requires when the link is and is not enabled (i.e. only the PHY is powered) as well as the total power required by the node. PDM obtains this information via the node;s power distribution management registers. Power information is maintained by the PDM and is used to build a power allocation map.

Once a node's power information has been enumerated, the PDM turns the nodes link-off. - only the PHY may remain enabled to consume cable power. In a like manner, each cable-powered node on the bus will have its power requirements enumerated and stored in the appropriate power domain management structures by the PDM. Once all power domain structures have been created, the serial bus is ready for transaction packet processing – the PDM transmits a link-on PHY configuration packet to a cable-powered node upon receipt of a message request command packet 01_{16} "Node Power Enable". A node containing a software application targeted for the device node to be enabled may initiate the "Node Power Enable" message request command packet.

There are no mechanisms by which the PDM may determine the amount of power a node's PHY consumes versus the amount of power required by the rest of the node components. Therefore, cable-powered nodes consuming 3 watts or less, including their link, are not required to have their link turned off – the PDM allocates 3 watts for each cable-powered node regardless of whether its link is enabled.

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4.1.2.1 Power State Control

Once the PDM has allocated power to a cable-powered node, the node's power policy owner manages power state transitions. The node's power policy owner manages the amount of power consumed by the node at any instance in time. Prior to a power consumer "disabling its link"[1], the cable-powered node shall notify the PDM of such action transmitting either a message request command 01_{16} or 04_{16} – "Link Off, Maintain Node Power Allocation", or "Link Off, Release Node Power Allocation, Maintain PHY Power Allocation", respectively.

Only the PDM shall update the power domain allocation map, i.e. the PDM is the only mechanism by which power shall be allocated from/to the power domain allocation map or to/from a cable-powered node.

Message request and message response packets shall be used to determine when a cable-powered node is to have its power state altered (i.e. link-on, link off, suspend, standby, resume and restore - with adjustments made, as appropriate, to the power domain allocation map).

[1]"disabling its link" refers to a process that results in the "L" bit equal to zero in the node's self-ID packet.. A new PDM may be instantiated on serial bus at any time. The new PDM shall, after enabling the link of the cable-powered node, read the node's "*valid*" bit in its NODE_POWER register to determine if the node had been managed by the previous PDM.

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5. Power Distribution Manager

The power distribution manager (PDM) shall be a bus manager-capable node that has the pmc bit set in the bus information block, as specified by IEEE Std 1394a-2000. A PDMS compliant node shall be a DEP capable node as defined in IEEE P1394.1 Annex C "Discovery and Enumeration Protocol.

When contending to become bus manager, a node that has its pmc bit set shall be the bus manager.

The PDMS compliant node, after noting that the current bus manager does not have its pmc bit set, shall set the abdicate bit in the STATE_SET register of the current bus manager. A PDMS compliant bus manager shall ignore its own incumbency and behave as if it were a challenger for the role of bus manager.

The PDMS compliant node shall then initiate a serial bus reset.

Immediately upon completion of the self-identify process, the PDMS compliant node shall attempt to become the bus manager in accordance with the procedures in IEEE Std 1394-1995, with one exception: The PDMS compliant node shall not wait 125 ms, rather, the PDMS compliant node will wait 100 ms before making a lock transaction to the BUS_MANAGER_ID register at the isochronous Resource Manager node. The PDMS compliant node shall attempt to become the bus manager 100 ms after completion of the self-identify process.

If the PDMS compliant node fails to become the bus manager, it shall test the pmc of the current bus manager. If the pmc bit of the current bus manager is set, this algorithm terminates and the current bus manager becomes the PDM. If the pmc bit of the current bus manager is not set, the PDMS compliant node shall transmit a PHY configuration packet with the *R* bit set to one, the root_*ID* field set to a value of $3F_{16}$, and the *T* bit cleared to zero. The effect of this PHY configuration packet is to clear the force_root bit of all nodes to zero while leaving the gap_count at its present value.

The PDMS complaint node shall then initiate a serial bus reset and attempt to become the bus manager as described above.

The PDM executes power manager responsibilities after first fulfilling the obligations of a bus manager specified by IEEE Std 1394-1995 and DEP obligations as defined in IEEE P1394.1 Annex C "Discovery and Enumeration Protocol".

5.1 Power Distribution Manager responsibilities

PDM responsibilities include:

a) Power domain management (allocating and deallocating cable power from power providers)

b) POWER_SOURCE register updates for cable-powered nodes

c) PDM_ID register updates for cable-powered nodes

d) Discovery Proxy for cable-powered managed nodes

e) Optionally, Discovery proxy for self-powered nodes

f) Optionally, the PDM may perform service and function proxy tasks as defined in IEEE P1394.1 Annex C "Discovery and Enumeration Protocol".

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5.1.1 Managing power domains

After a bus reset event and before the PDM responds to any message requests, the PDM must determine the amount of power available in each power domain and the total amount of power requested by all cable-powered nodes in each power domain.

The actions taken by the PDM subsequent to a bus reset are based on a requirement that a cable-powered node, upon becoming attached to the serial bus, shall have its link powered off and have it remain off until a link-on PHY configuration packet is received. Cable-powered nodes that consume 3 watts or less with their link enabled are not required to disable their link. The PDM allocates 3 watts for each cable-powered node - regardless of whether its link is enabled.

After a bus reset, the PDM shall perform the following actions:

- Parse the serial bus topology into disjoint power domains.
    - The PDM may obtain needed information from the repeat power bit in the POWER_CLASS field of each node's self_ID packet. The repeat power bits may show the limits of the power domains. Information read from configuration ROM shall take precedent over other means that could be used to parse the disjoint power domains on the serial bus.
- The PDM calculates the amount of power available in each power domain.
- Within each power domain, the PDM uses information in the node self-ID packets to determine the total amount of power required for cable-powered nodes in each power domain. The PDM must reserve at least 3 watts for every cable-powered node in the power domain.
- The PDM transmits a link-on PHY configuration packet to the first cable-powered node, i.e. the cable-powered node with the lowest node-ID
- The PDM then enumerates the precise power requirements for the node by reading the appropriate information from the node CSR space.
- The PDM disables the nodes link.
- The previous three steps are repeated for each cable-powered node in each power domain.

Once node power requirement enumeration is complete, the PDM is ready to process power distribution message request transactions.

5.1.2 Managed and Unmanaged Nodes

Power providers that are incapable of responding to DEP message packets and that do not contain a Node_Power_Directory entry in the root directory of their configuration ROM, are not compliant with this specification and are discouraged.

System providers implementing a mixture of 1394 socket types shall provide information in the Node Power directory that describes the socket attached to each port. Node power directory data structure and data contents are defined in subsequent sections of this specification.

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The PDM shall be the discovery proxy for all PDMS complaint cable-powered nodes. Non-PDMS compliant cable-powered nodes (Legacy nodes) shall be sent a link-on PHY configuration packet by the PDM and left on by the PDM.

There are opportunities for PDMS complaint nodes to perform a service, or function proxy for a Legacy cable-powered node. A service proxy may turn off (disable) the link but it shall not enable the link of a Legacy node – only the PDM shall enable the link of a node. A PDMS compliant capable-powered node may enable its own link if power has previously been allocated to the node.

A Legacy service proxy node may not disable the link of a Legacy node until successfully transmitting a message request command of either 01_{16} or 04_{16} – "Link Off, Maintain Node Power Allocation", or "Link Off, Release Node Power Allocation, Maintain PHY Power Allocation", respectively, to the PDM. When the PDM receives either of these message request commands, the PDM shall assume the Legacy node's link is off.

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6. Power distribution management process and procedure

Message request/response packets are used by PDM to perform the tasks associated with distributing and allocating power to cable-powered nodes. These protocols are used when cable-powered nodes alter their power consumption requirements or power state. This section provides examples of how these protocols are used.

6.1 Node power allocation change

Peak power, defined as transient power (P_t), and normal operating power, defined as quiescent power (P_q), requirements of a node are managed during the power distribution management process through the use of the message request/response packet protocols defined in this specification.

When the P_t requirement of a node exceeds its P_q requirement, the *node power manager* shall initialize register `Node_Power_Required` to the node's P_t value. The supplier of a PDMS compliant device node shall configure the PHY for a self-ID power class field appropriate to the node's P_t.

When the node power requirement transitions to P_q, the node's power manager shall set the value of register `Node_Power_Required` to P_q and, subsequently, transmit a message request command of either 02_{16} or 03_{16} – "Deallocate" or "Allocate", respectively. The message request command provides the PDM with a value (in deciwatts) of the amount of power change requested by the node.

When a message request command is for an additional amount of power (Allocate), the PDM determines if the requested amount of power is available in the power domain. If power is available, the PDM shall write the new value for the amount of power allocated to the node's `Node_Power` register. If there is insufficient power, the PDM will respond with a write to the requesting nodes message response register with an error code value of 01_{16} – Insufficient power available.

A message request command for a decrease (Deallocate) in the amount of power required for the node shall result in the PDM updating the value in the node's `Node_Power` register to match that required by the node. The PDM increases the amount of power available in the power domain by an amount equal to the power change value provided in the message request.

The following example is applicable for any instance of a change in a node's power requirements:

> *A device node with a P_t of 8 watts and a P_q of 2 watts shall have a self-ID power class of 111_2 (node is consuming 3 watts and needs an additional 7 watts) and a `Node_Power_Required` register value of 80 deciwatts. Upon receipt of a link-on and when ready to process transaction packets, the node shall transmit a ping packet addressed to itself.*
>
> *A PDMS compliant node will not respond to any packet (other than a link-on PHY configuration packet) until its `POWER_SOURCE`, `PDM_ID` and `Node_Power` registers have been initialized or until 125 milliseconds has expired since completion of transmitting the required ping packet following receipt of a link-on.*
>
> *When an active PDMS complaint node contains power on default values for its `POWER_SOURCE`, `PDM_ID` and `Node_Power` registers it is deemed to be functioning on a Legacy serial bus, that is, a serial bus that does not contain a PDMS complaint Bus Manager.*
>
> *When the PDM detects self-ID from the ping packet, the PDM sets the `Node_Power` register to the value it reads from the `Node_Power_Required`*

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register - 80 deciwatts (the amount of P_t required by the node). NOTE: The self-ID packet identified a power class requiring an additional 7 watts, however, the `Node_Power_Required` register provides a finer granularity of actual required power. In this instance, an additional 5 watts over the 3 watts allowed for cable-powered PHY - a total of 8 watts.

PDM sets the `POWER_SOURCE` register to the node-ID of the power provider designated by the PDM to be the source of the node's power – this establishes the power domain for the cable-powered node. PDM writes its own node-ID into the `PDM_ID` register. PDM subtracts from the total amount of power available in the power domain by the value set in the `Node_Power` register.

The power class field in the node's self-ID packet specifies the maximum amount of power a node may consume (inclusive of power consumed by the PHY when the link is not enabled). The value contained in the `Node_Power_Required` register may be greater than that specified by the nodes self-ID power class field. In this instance, the node shall not consume its required amount of power until after the `Node_Power` register has been set to a value equal to that of the `Node_Power_Required` register.

When the example node reaches its quiescent power state, the node's power manager sets the value in the `Node_Power_Required` to 20 deciwatts – the required P_q for the node. The node power manager then writes a message request command 02_{16} (Deallocate) containing a power change value of 60 deciwatts to the message request register of PDM. PDM responds with a write to `Node_Power` with a new value of 20 deciwatts. PDM increments the total power available in the power domain by 6 watts. A message request command of 03_{16} (Allocate) whose change in power value results in a request for an amount of power greater than an amount available in the power domain shall result in PDM writing a message to the message response register of the message initiator with an error code of 01_{16} - Insufficient Power Available.

Unless the "L" bit in its self-ID packet would change from one (1) to zero (0), there is no requirement for a serial bus power consumer node to generate a message request command for a power allocation change message when a change to power allocated to the node is not required. A serial bus power consumer node may change the amount of power it consumes in the range of zero to the value contained in register `Node_power` without sending a message request command packet to the PDM. When a change to the amount of power allocated to the node, that is the value contained in register `Node_power` is changed, a serial bus power consumer node shall send a message request command packet to the PDM with the value of the power allocation change.

When a request for an increase in power allocation specified in the message request command packet exceeds the total amount of power required by the node as defined in the `Node_Power_Required` register, the PDM shall respond with a message response packet containing an error code value of 03_{16} – Illegal Parameters.

When an increase in the amount of power allocated to a node is required, the node manager shall adjust the value of the `Node_Power_Required` register followed by a write to the message request register of the PDM with a command value of 03_{16} ("Allocate"). The value of the increase in power to be allocated to the cable-powered node shall be identified in the message request packet.

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A message request command of 03_{16} (Allocate) whose change in power value results in a request for an amount of power greater than the amount available in the power domain shall result in the PDM writing a message to the message response register of the message initiator with an error code of 01_{16} - Insufficient Power Available.

When a decrease in the amount of power allocated to a node is required, the node manager shall adjust the value of the `Node_Power_Required` register followed by a write to the message request register of the PDM with a command value of 02_{16} ("Deallocate"). The value of the decrease in power allocated to the cable-powered node shall be identified in the message request packet.

A message request command of 00_{16} (Link Off, Maintain Node Power Allocation) is neither a request for an increase or decrease in power allocation to the cable-powered node. A 00_{16} command notifies the PDM that the cable-powered node link will be disabled and that the PDM shall continue to allocate the power previously allocated to the cable-powered node.

A cable-powered node whose link has been previously enabled shall not arbitrarily disable and enable its own link. Once a cable-powered node has had its link enabled, it shall remain enabled until the cable-powered node (or its proxy) sends a message request command to the PDM that contains about the power being allocated to the node (no change or decrease) – thus notifying the PDM that the node's link is being disabled and whether some or all of the power currently allocated to the node may be reallocated to the power domain power allocation map or power currently allocated to the node shall continue to be allocated to the node.

6.2 PDM transition Power Domain and PDM_ID initialization

A newly connected bus manager/PDM capable node shall not disrupt power consumer nodes that have their link enabled or have power allocated to them (regardless of the state of their link). PDM_ID registers containing the node-ID of the previous PDM shall be replaced with the node-ID of the new PDM by the new PDM. The Power Allocation Map for the new PDM shall be established based upon values contained in the `Node_Power`, `Node_Power_Status` and `Node_Power_Required` registers of the able-powered nodes present on serial bus.

6.3 Power providers without a link layer

A power provider that does not have a link or, if it has a link, does not have a node power directory entry or a power distribution management entry in the root directory of its configuration ROM is a Legacy Power Provider. The PDM shall determine the total power capability of a Legacy Power Provider from the power class field of its self-ID packet. The PDM is not able to determine the power delivery status for each port of a Legacy Power Provider nor is it able to determine cable power loss. Legacy Power Providers are discouraged.

PDMS compliant power providers have mechanisms that the PDM may use to determine cable power loss.

For example, the PDM may determine the power consumption status of power consumers in a leg of a power domain serviced by a port on a PDMS compliant power provider. The PDM may determine cable power loss in that leg by subtracting the sum of all power being consumed by consumers in that leg from the power delivery status of the port servicing that leg. Port power delivery status is obtained via the response received from a message request command 05_{16} – "Node Power Source Status Request".

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6.4 Enabling a cable-powered node

A node executing an application requiring the service of a particular function of a cable-powered node may, upon discovery of the required function in a cable-powered node, send a message request command 01_{16} ("Node Power Enable") to the message request register of PDM. The message request data contains the node-ID and/or the EUI-64 of the cable-powered node. NOTE: The PDM executes discovery proxy service for all cable-powered nodes that do not have their link enabled.

The PDM shall support node activation mechanisms as specified in IEEE 1394.1 Annex C - Discovery and Enumeration Protocol.

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7. Power distribution management registers

This section defines several different types of registers, all of which are necessary to support power distribution management on Serial Bus:

- Registers for PDMS compliant power providers,
- Registers for PDMS compliant cable-powered nodes

7.1 Power Distribution Management registers

The Power Distribution Manager (PDM) is a Bus Manager-capable node that implements extensions to the standard registers defined by IEEE Std 1394-1995. Specifically, PDM shall implement the abdicate and `pmc` bits as defined in IEEE Std. 1394a-2000. In addition, PDM implements several new registers. These registers shall lie within initial units space and shall be located at or above address FFFF F001 0000_{16} within the node's 48-bit address range.

7.1.1 Power Consumer Node Registers

Each power consumer node shall have the set of control and status registers shown in the following table. These registers shall lie within initial units space and shall be located at or above address FFFF F001 0000_{16} within the node's 48-bit address range.

The relative relationship of these registers is fixed within a contiguous block of quadlets, as defined by the table below.

Table 7-1 Power Consumer Node PDM Registers

Relative offset	Name	Description
00_{16}	`Node_Power_Status`	Reports the node's current power consumption status (in deciwatts)
04_{16}	`Node_Power`	Amount of power allocated to the node (in deciwatts)
08_{16}	`Node_Power_Required`	Amount of power required for full node (all units) functionality (in deciwatts)
$0C_{16}$	`PDM_ID`	Node-ID of the PDM for this node (Bus Manager Node-ID)

The base address of each node's set of power distribution management registers is obtained from the PDM_Registers entry in the Node Power Directory pointed to by the Node_Power_Directory entry in the root directory of the node's configuration ROM.

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7.1.1.1 Node_Power_Status register

PDMS compliant nodes shall implement the Node_Power_Status register.

The Node_Power_Status register contains the value of the actual amount of power (in deciwatts) being consumed by the cable-powered node at the time the register is read. A read of this register may initiate an update to its current value.

The format of `Node_Power_Status` register in the power distribution management register set is shown in the following figure.

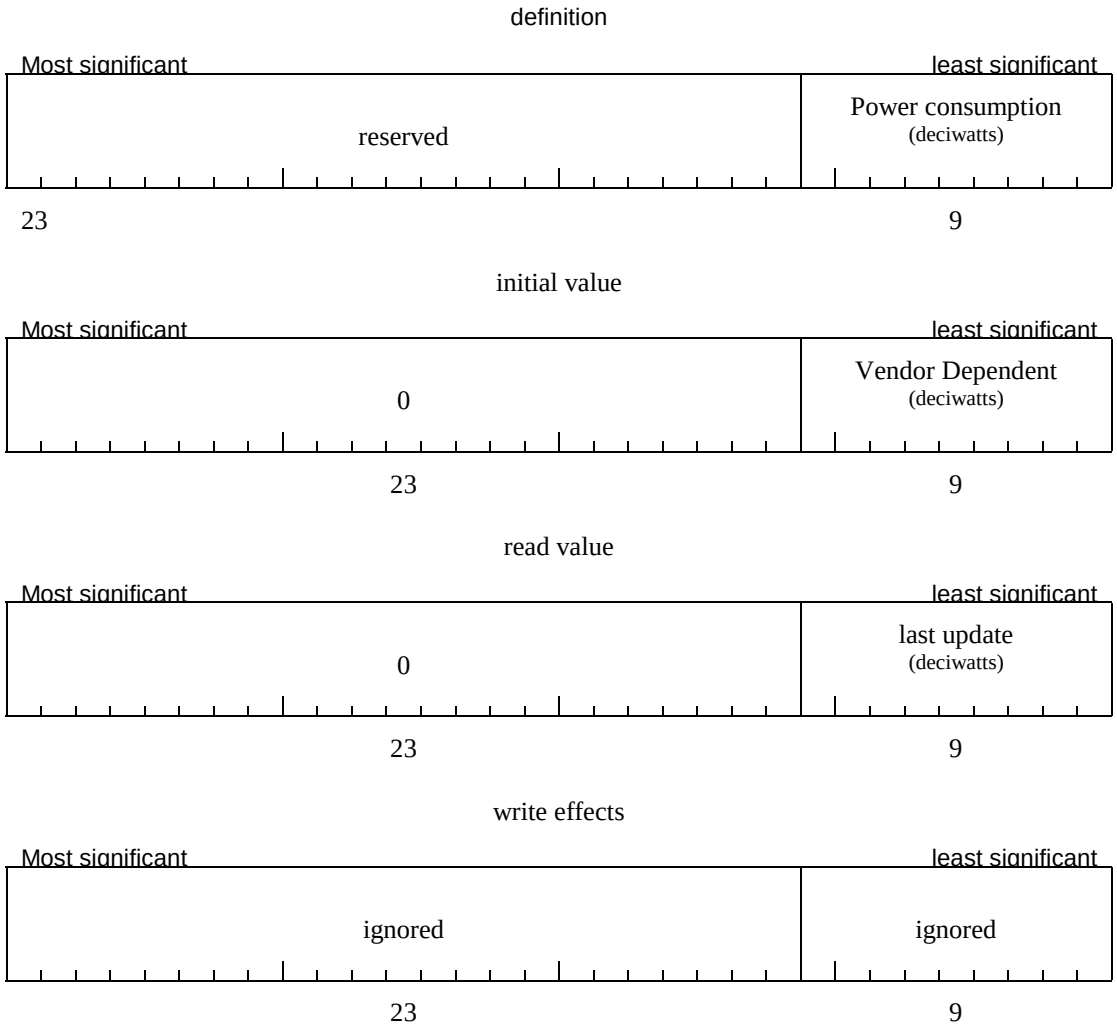

Figure 7-1 Node_Power_Status register

Serial bus write transactions to the `Node_Power_Status` register shall not change the value contained in the `Node_Power_Status` register.

Only the node manager shall update the value in the `Node_Power_Status` register.

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A serial bus read transaction packet addressed to a node's `Node_Power_Status` register shall result in a response containing the current value held in the node's `Node_Power_Status` register. A read of this register may initiate an update to its current value.

7.1.1.2 Node_Power register

The `Node_Power` register contains the value of power currently allocated to the node by the PDM. The format of the register is shown in the following figure.

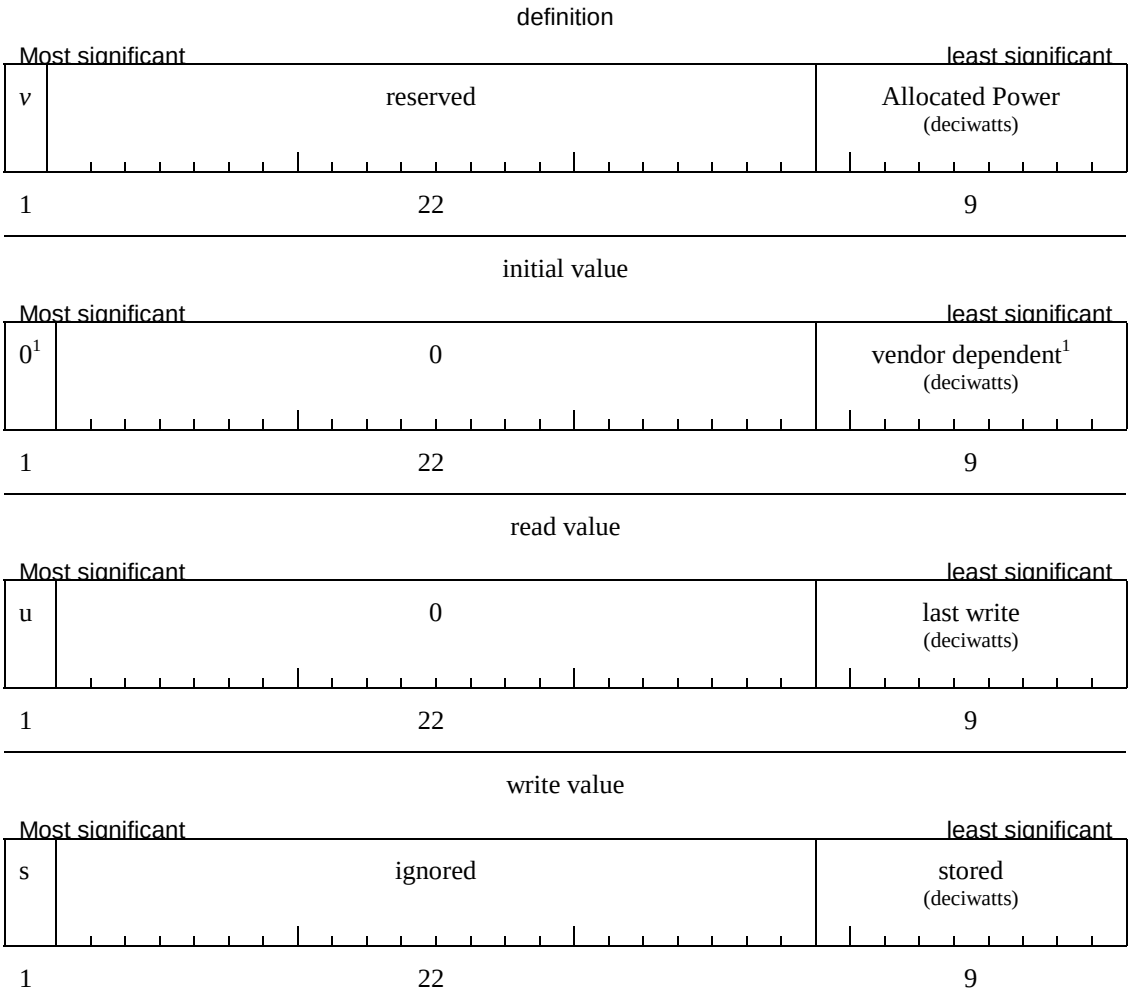

Figure 7-2 Node_Power register

When the *valid* bit (abbreviated *v* in the above figure) is set to one, the value contained in the field *Allocated Power* is valid. The *valid* bit is set to one by the PDM when the PDM updates the *Allocated Power* field.

Writes to the `Node_Power` register by the node power manager shall not change the value contained in the `Node_Power` register.

Only the PDM shall update the value in the `Node_Power` register using serial bus write transaction packets.

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The node manager shall be able to read the value in the Node_Power register.

[1]The value for field *valid* (abbreviated *v* in the table) shall be set to zero upon power-on reset. Upon a link off transaction the *v* bit and the *Allocated Power* field may either be set to 0 or retain their current value depending on whether the cable-powered node has requested the PDM to release its allocated power or not. If the PDM maintains power allocation to the node after the node's link is disabled, the *v* bit and the *Allocated Power* field values shall retain their current value.

7.1.1.3 Node_Power_Required register

The Node_Power_Required register contains the value of the power allocation being requested by the cable-powered node. The format of the register set is shown in the following figure.

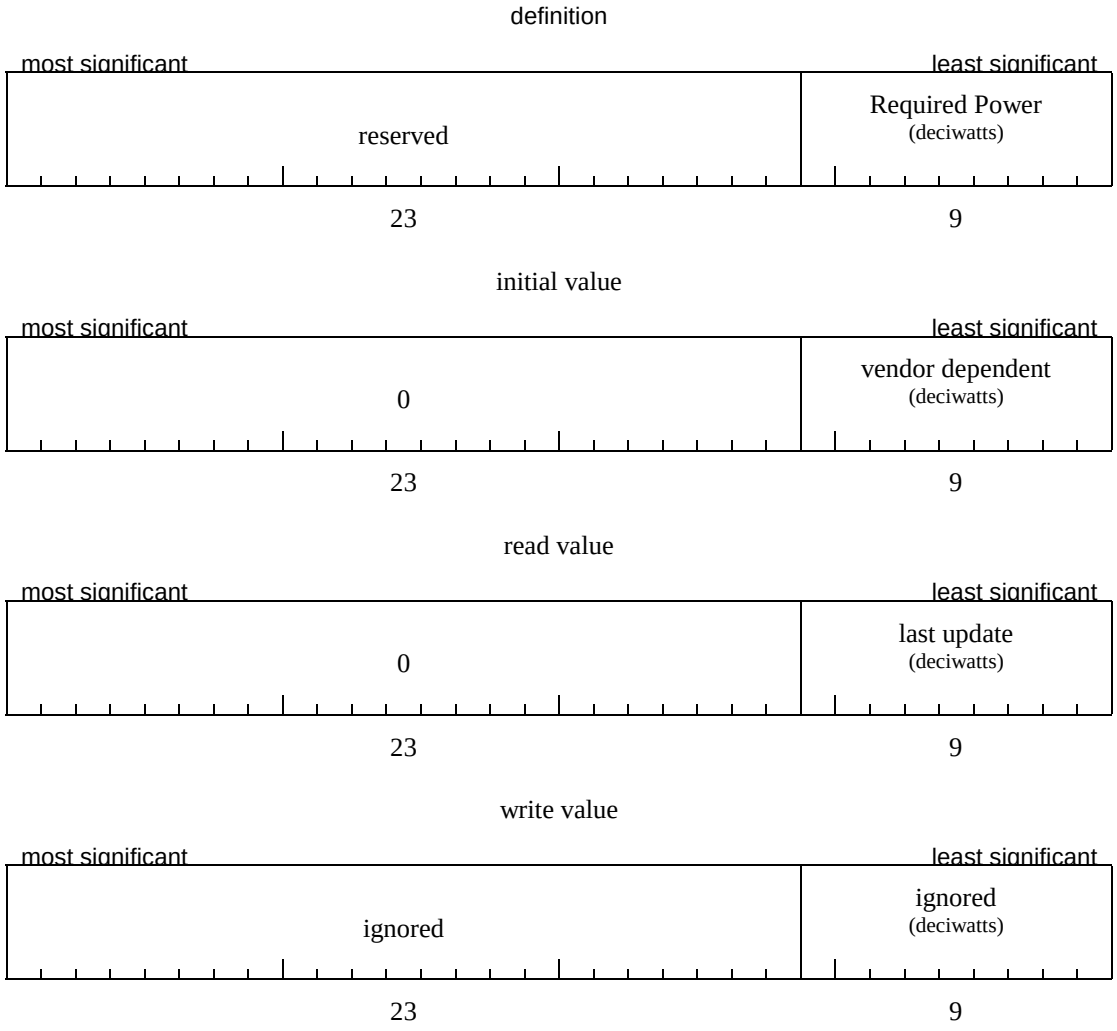

Figure 7-3 Node_Power_Required register

Writes to the Node_Power_Required by serial bus write transaction packets shall not change the value contained in the Node_Power_Required register.

Only the node manager shall make updates to the Node_Power_Required register.

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A serial bus read transaction packet addressed to a node's `Node_Power_Required` register shall result in a response that contains the current value held in the node's `Node_Power_Required` register.

7.1.1.4 POWER_SOURCE and POWER_FAIL_IMMINENT registers

Though traditionally reserved for back-plane environment implementations, PDMS compliant cable-powered nodes shall implement the POWER_SOURCE and POWER_FAIL_IMMINENT register as defined in clause 8.3.2.3.3 and 8.3.2.3.4 of IEEE Std. 1394-1995.

PDM sets the POWER_SOURCE register to the node-ID of the power provider designated by the PDM to be the source of the node's power – this establishes the power domain for the cable-powered node.

A PDMS compliant power provider shall issue a broadcast write transaction to serial bus POWER_FAIL_IMMINENT register address prior to removing power from serial bus.

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7.1.1.5 PDM_ID register

The format of PDM_ID register in the power distribution management register set is shown in the following figure.

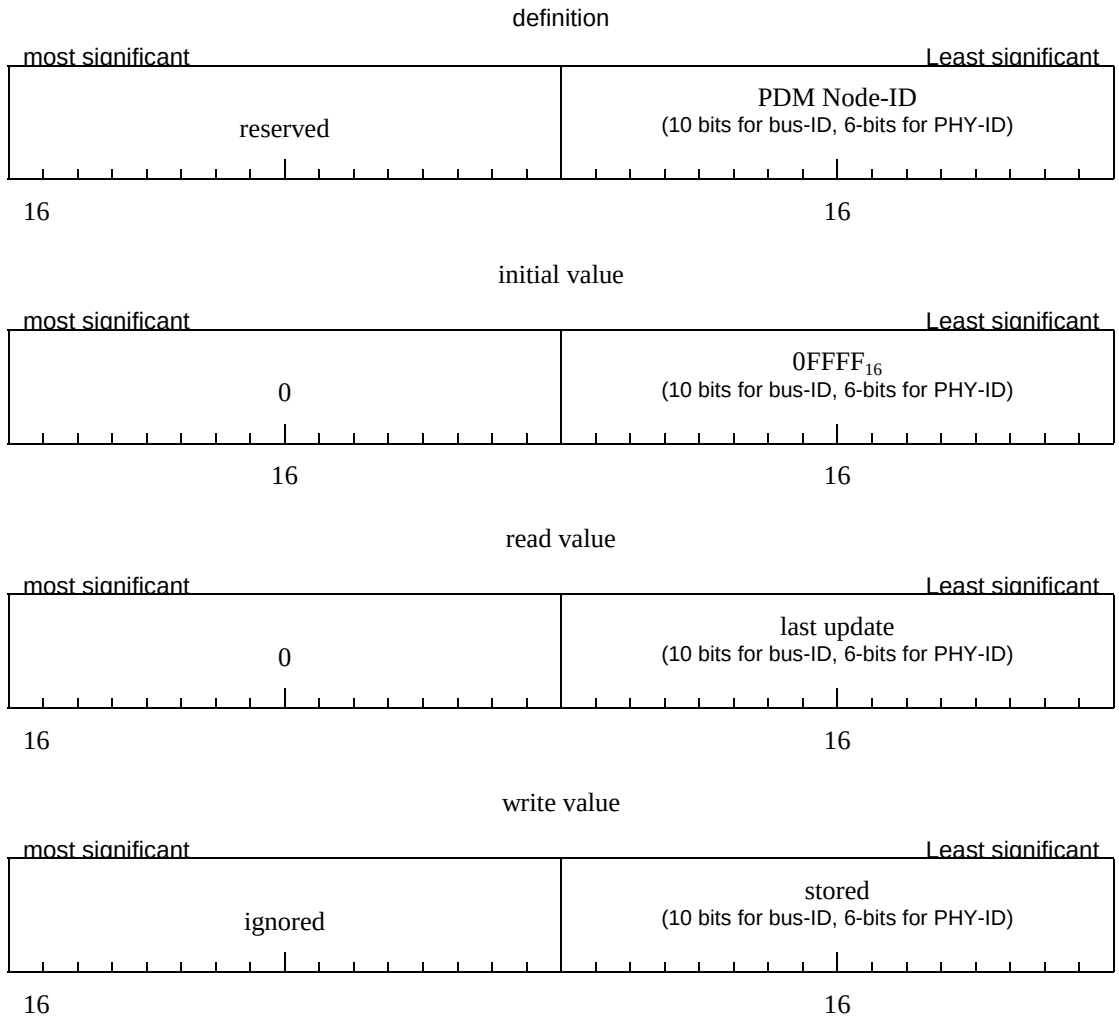

Figure -7-4 PDM_ID register

Writes to the PDM_ID by the node power manager shall not change the value contained in the PDM_ID register.

Only the PDM shall update the PDM_ID register via serial bus write transaction packets.

The node manager shall be able to read the value in the PDM_ID register.

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8. Configuration ROM

All PDMS complaint nodes shall implement a general format configuration ROM in accordance with IEEE P1212 and IEEE Std 1394-1995 and its amendments. The bus information block and root directory are at fixed locations; all other directories and leaves are addressed by entries in their parent directory.

The figure below illustrates the general ROM format accommodation for a diversity of directory and leaf entries in a tree structure. The root directory in all PDMS compliant nodes shall contain a Node_Power_Directory entry consisting of an Extended Key Specifier ID, Extended Key, and Node Power Leaf. A PDMS compliant cable-powered node shall contain a Node PDM Registers entry in the Node Power Directory.

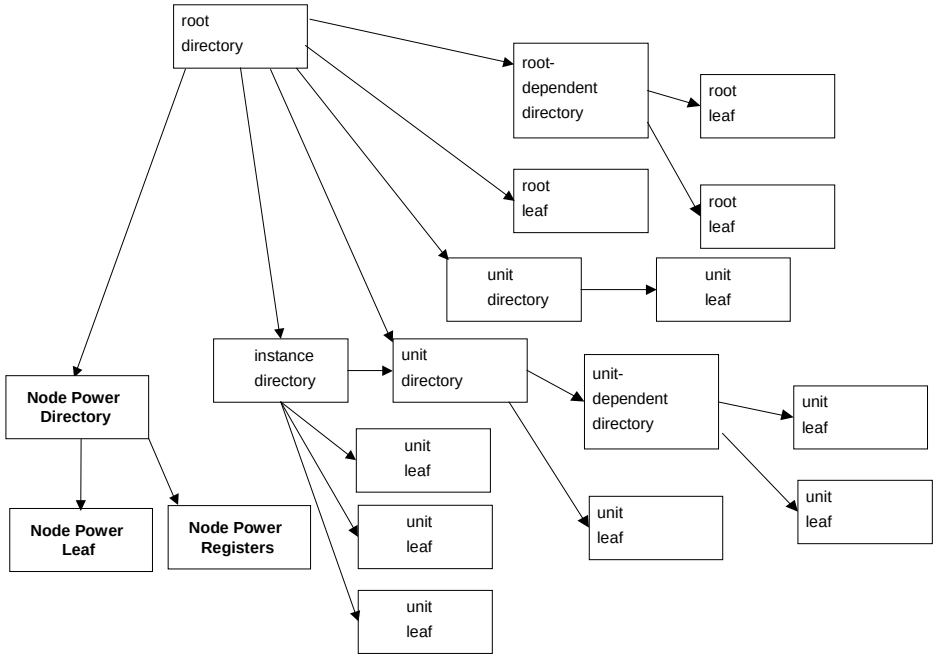

Figure 8-1 Configuration ROM hierarchy

The value for the Extended Key Specifier ID shall be $0050F2_{16}$.

The value for the Extended Key shall be $00000A_{16}$.

8.1 Bus Information Block

Power Managers shall implement a bus information block at a base address of FFFF F000 0404_{16}. For convenience of reference, the format of the bus information block defined by IEEE Std 1394-1995 is reproduced below along with extensions defined by its amendment, IEEE 1394a.-2000.

The pmc bit, an extension defined by 1394a-2000, defines whether the node is Power Manager capable or not.

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most significant

31_{16} (“1”)						33_{16} (“3”)	39_{16} (“9”)		34_{16} (“4”)		
irmc	cmc	isc	bmc	pmc	r	cyc_clk_acc	max_rec	r	g	R	lnk_spd
node_vendor_ID									chip_ID_hi		
chip_ID_lo											

least significant

Figure 8-2 Bus Information Block

PDMS compliant nodes may set the `bmc` bit to one; indicating the node is bus manager capable.

PDMS compliant nodes that are bus manager capable and PDM capable shall set their `pmc` bit to one – indicating the node is Power Distribution Manager capable.

8.2 Node_Power_Directory Entry in the Root Directory

The Node_Power_Directory entry is specified using the extended key architecture as defined in IEEE P1212 clause 7.5.2. The Node_Power_Directory entry consists of the following three root directory entries:

Table 8-1 Node_Power_Directory root directory entries

Key	Name	Description
$1C_{16}$	`Extended Key Specifier ID`	identity of the organization defining the following extended key
$1D_{16}$	`Extended Key`	Extended key defined for this specification
$0DE_{16}$	`Node_Power_Directory`	unsigned offset of directory within configuration ROM (relative to this address)

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The format for the Node_Power_Directory entry is illustrated in the following figure:

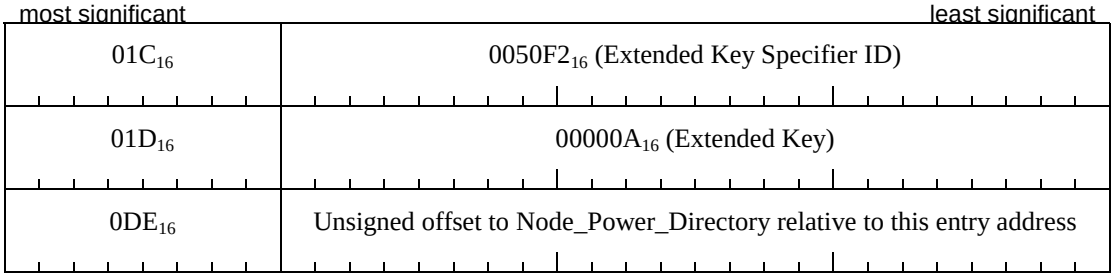

Figure 8-3 Node_Power_Directory values

8.2.1 Node Power Directory

PDMS compliant nodes provide a Node Power Directory consisting of the following entries:

Table 8-2 Node Power Directory entries

Key	Name	Description
012_{16}	`Specifier ID (0050F2`$_{16}$`)`	identity of the organization defining this directory
013_{16}	`Version (00000A`$_{16}$`)`	version number of the definition of this directory
$0B0_{16}$	`Node_Power_Leaf`	unsigned offset of leaf information within the configuration ROM (relative to this address)
070_{16}	`PDM_Registers`	unsigned CSR offset of PDM registers within Units memory space from base address FFFF F000 0000_{16}
031_{16}	`Node_Power_Capability`	power available from the power provider in deciwatts
003_{16}	`Vendor`	OEM Unique Identifier defining power use model three
017_{16}	`Model`	OEM model number specified by the above vendor
$03E_{16}$	`Alternate Power Management Specifier`	Unique Identifier defining power use model two
$03F_{16}$	`Alternate Power Management Version`	Version number specified by the above unique specifier

All PDMS compliant nodes shall implement Node Power Directory entries for:

- Specifer ID
- Version
- Node Power Leaf

All PDMS complaint power providers shall implement Node Power Directory entries for:

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- Node_Power_Capabilities

All PDMS complaint power consumers shall implement Node Power Directory entries for:

- PDM_Registers

The format for the entries in the Node Power Directory is illustrated in the following figure:

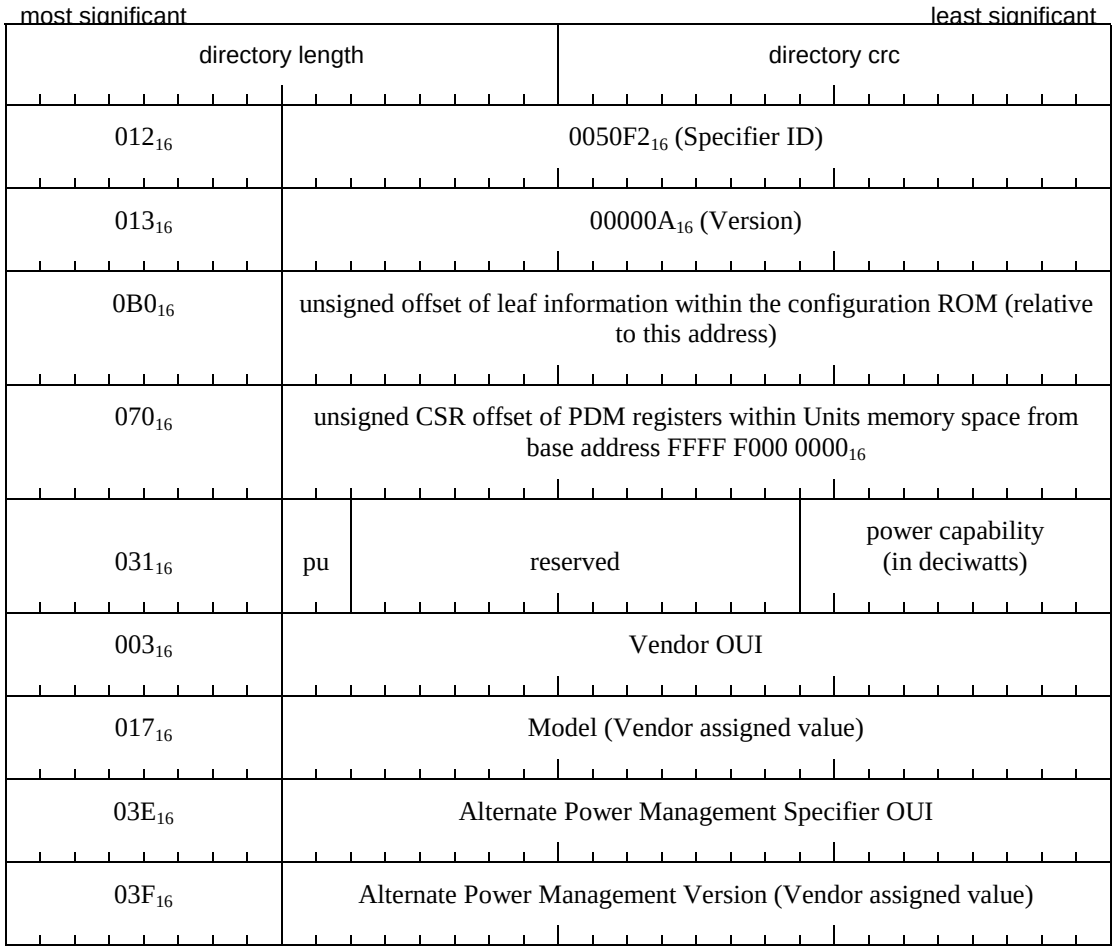

Figure 8-4 Node_Power_Directory values

8.3 Node_Power_Leaf Entry

All PDMS compliant nodes shall contain one Node_Power_Leaf entry in the node power directory of their configuration ROM. A node that is neither a power consumer, a power provider, nor capable of being the PDM is PDMS compliant when this entry exists in its node power directory and the associated leaf exists in its configuration ROM.

A Node_Power_Leaf entry is located in the node power directory. The Node_Power_Leaf entry specifies the specific location of the leaf in the node power directory as (4 * (*value* of Node_Power_Leaf)) + (Node_Power_Leaf entry address).

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The format of this entry is illustrated in the following figure:

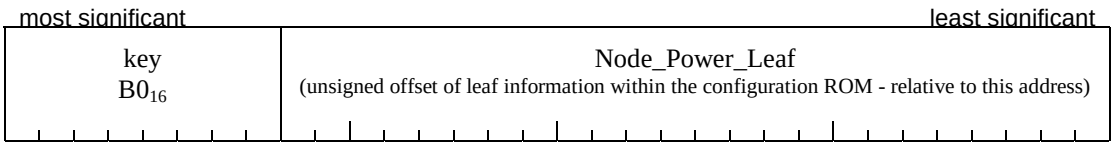

Figure 8-5 Node_Power_Leaf entry

The format of the Node Power Leaf conforms to IEEE P1212 clause 7.5.3 and is illustrated in the following figure:

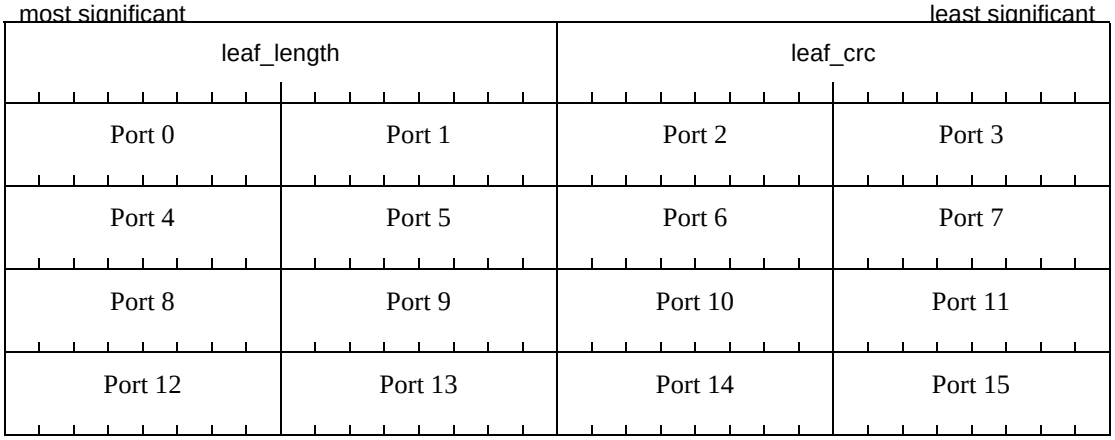

Figure 8-6 Node Power Leaf entries

The number of quadlets in the node power leaf (leaf_length) shall be a value between one and four and is dependent upon the number of ports implemented by the node.

The leaf_crc conforms to definition specified in IEEE P1212.

The value for each port entry in the node power leaf defines the characteristics of that port. Port characteristics are defined in the following figure:

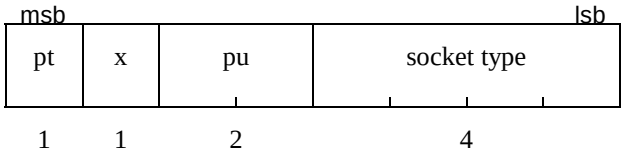

Figure 8-7 PDM_Registers entry

Power pass through (abbreviated *pt* in preceding figure) shall be one when the Vp socket pin for this port contains a source of serial bus cable power and connects to the Vp socket pin of one or more sockets that may be connected to other ports in this node. This bit shall be zero when the Vp socket pin for this port has no connection with a Vp pin on any other port in this node.

External (abbreviated *x* in the preceding figure) shall be one when the device containing this port has a socket connected to the port that is capable of connecting an external serial bus cable. This bit shall be zero when the device containing this port does not have a socket connected to the port capable of connecting an external serial bus cable.

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Power Use Model (abbreviated *pu* in the preceding figure) specifies the type of power available to serial bus from this port. Valid values for the Power Use Model field are defined in the following table:

Table 8-3 Power Use Model Values for Sockets

pu value	power source description
0	No power is provided by this port (power provided by any other port is passed through this port)
1	1394 cable power is available from this port (a Node_Power_Capablity entry shall be in the root directory for power use model one).
2	Power on this port is managed by an Alternate Power Management specification - not a 1394 serial bus PDM. (a Node_Power_Capability entry may be in the node power directory for power use model two). This specification does not address power distribution management for an Alternate Power Management specification. The Alternate Power Management Specifier OUI and Alternate Power Management Version entries in the node power directory define the specification for the Alternate Power Management specification.
3	Power is provided to this port by a Vender specified power source – not a 1394 serial bus cable power provider. (a Node_Power_Capability entry may be in the node power directory for power use model three). This specification does not address power distribution management for a Vendor defined power source. The specification for a Vendor defined power source is defined by the Vendor OUI and Model entries in the node power directory.

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The *Socket type* field specifies the type of 1394 socket attached to the port as defined in the following table:

Table 8-4 Socket Types

VALUE	SOCKET TYPE	DEFINED IN STANDARD
0000_2	No socket present	N/A
0001_2	4-pin copper	IEEE 1394a-2000
0010_2	6-pin copper	IEEE 1394-1995
0011_2	9-pin beta copper	IEEE P1394b
0100_2	9-pin bilingual copper	IEEE P1394b
0101_2	Plastic optical fiber	IEEE P1394b
0110_2	Glass optical fiber	IEEE P1394b
0111_2	Hardened polymer clad fiber	IEEE P1394b
1000_2	CAT-5 copper (RJ-45)	IEEE P1394b
1001_2 thru 1101_2	Reserved	N/A
1110_2	Power Use Model Connector	Power Use Model Specification (see *pu* value 2 or 3)
1111_2	Unspecified	N/A

8.4 PDM_Registers Entry

PDMS compliant nodes shall contain a PDM_Registers entry in the node power root directory. of the node's configuration ROM. The PDM_Registers entry contains the number of quadlets offset from the base address of initial register space ($FFFFF0000000_{16}$) to the base address of the power distribution management registers for the PDMS compliant node.

There shall be one PDM_Registers entry in the node power directory.

The format of PDM_Registers entry is illustrated in the following figure:

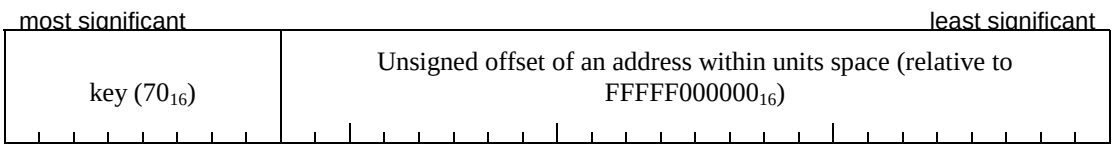

Figure 8-8 PDM_Registers entry

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8.4.1.1 Node_Power_Capability Entry

The Node_Power_Capability entry provides information about the power provider capabilities of the node. There is only one Node_Power_Capabiity entry in the node power directory.

The format of the Node_Power_Capability is illustrated in the following figure:

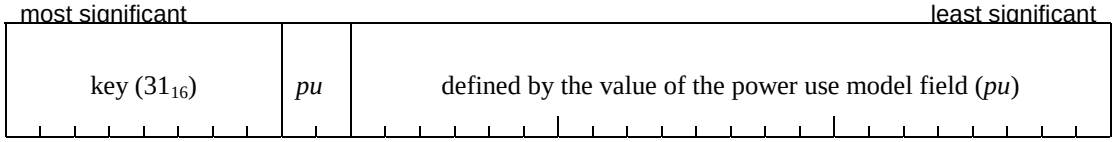

Figure 8-9 Node_Power_Capability entry

The power use model field (abbreviated *pu* above) defines the power use model of the power provider the Node_Power_Capability entry pertains to.

The valid values for the power use model bits are defined in the following table:

Table 8-5 Valid *pu* field values

pu Value	Definition
00_2	Reserved
01_2	1394 Cable Power Provider
10_2	Defined by an Alternate Power Management specification identified by the Alternate Power Management Specifier OUI and Alternate Power Management Version entries in the node power directory.
11_2	Defined by a Vendor power specification identified by the Vendor OUI and Model entries in the node power directory

Each power use model for a power provider shall be independent of the others. That is, if a node provides 1394 serial bus cable power and an vendor specific power source then power distribution events in the vendor specific power domain shall not affect the power provided in the 1394 serial bus cable power domain and vice versa.

The value for the least significant 22 bits is dependent upon the value of the power use model field as defined in the following figures:

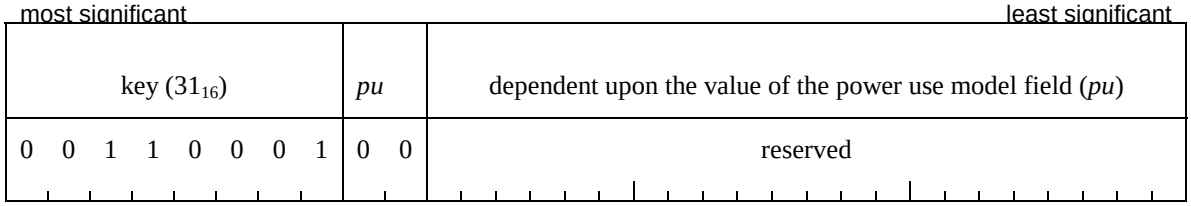

Figure 8-10 Power Use Model 00_2

Power use model 00_2 is reserved for future standardization.

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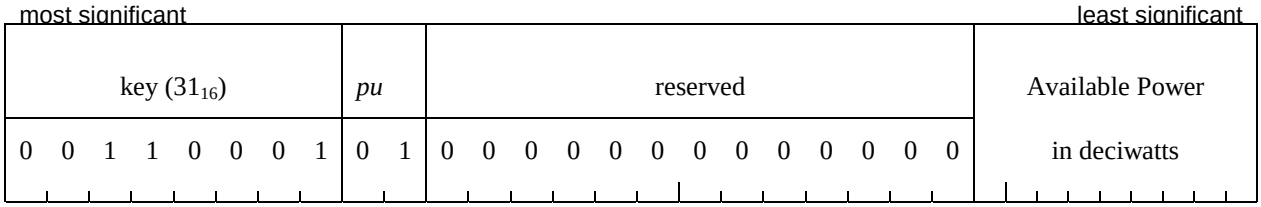

Figure 8-11 Power Use Model 01_2

The Available Power field defines the amount of power (in deciwatts) the provider is capable of providing to 1394 serial bus.

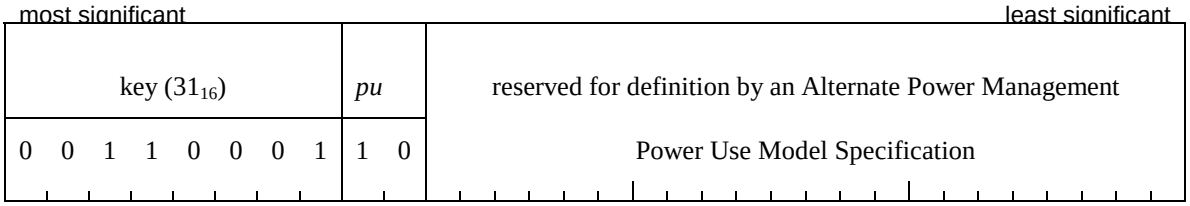

Figure 8-12 Power Use Model 10_2

The least significant 22 bits of power use model 10_2 is reserved for definition by an Alternate Power Management Specification identified by the Alternate Power Management Specifier OUI and Alternate Power Management Version entries in the node power directory.

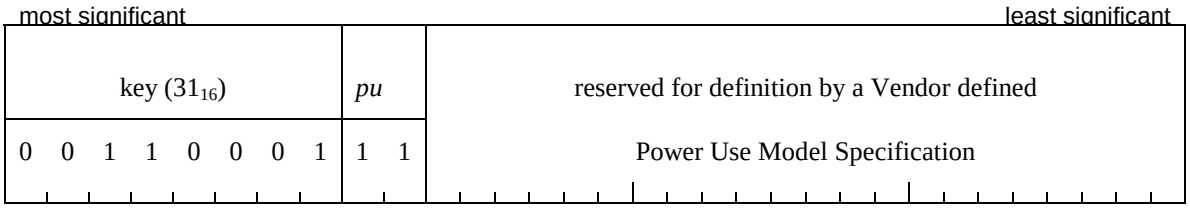

Figure 8-13 Power Use Model 11_2

The least significant 22 bits of power use model 11_2 is reserved for definition by a Vendor defined power use model specification identified by the Vendor OUI and Model entries in the node power directory.

8.5 Vendor OUI and Model Entries in the Node Power Directory

When the value of the power use model field (*pu*) in the Node Capabilities entry in the Node Power directory is 11_2, a PDMS compliant node may contain Vendor OUI and Model entries in the Node Power Directory. Vendor OUI and Model entries, when not present in the node power directory shall be taken from their values in the root directory.

Power provided to a node or port that is specified by a Vender specified power source shall not be a 1394 serial bus cable power provider.

The Vendor OUI identifies the organization or vendor that defines the specification for power use model 11_2 power sources. A PDMS compliant node may support power distribution management for power use model 11_2 as defined in the vendor identified specification. The value for the Model number entry in the Node Power Directory is vendor specific.

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The formats for the Vendor OUI and Model entries in the node power directory are illustrated in the following figure:

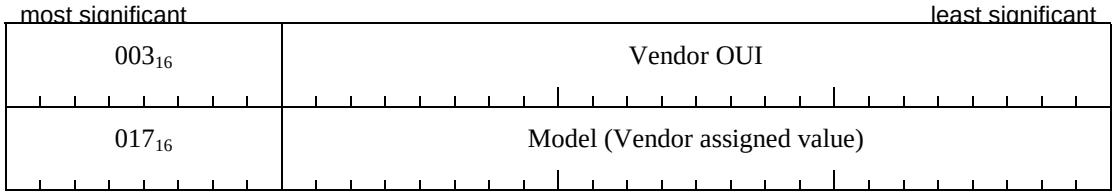

Figure 8-14 Vendor OUI and Model Entries - Node Power Directory

8.6 Alternate Power Management Specifier OUI and Version Entries

When the value of the power use model field (*pu*) in the Node Capabilities entry in the Node Power directory is 10_2, a PDMS compliant node shall contain Alternate Power Management Specifier OUI and Version entries in the Node Power Directory. When the Alternate Power Management Specifier OUI and Version entries are not present in the node power directory, power use model two shall not be used.

A node may be power managed by a power manager other than the PDM in a PDMS compliant node. The specification for an Alternate Power Manager shall be identified by the Alternate Power Manager Specifier Organizationally Unique Identifier (OUI) entry in the Node Power Directory. A node or port with a *pu* value of 11_2 shall not be managed by a PDMS compliant PDM.

The Alternate Power Management Specifier OUI identifies the organization or vendor that defines power distribution management for power use model 11_2. A PDMS compliant PDM may not support an Alternate Power Management Specification for power use model 11_2. The value for the Alternate Power Management Version entry in the Node Power Directory is vendor specific.

The formats for the Alternate Power Management Specifier OUI and Version entries in the node power directory are illustrated in the following figure:

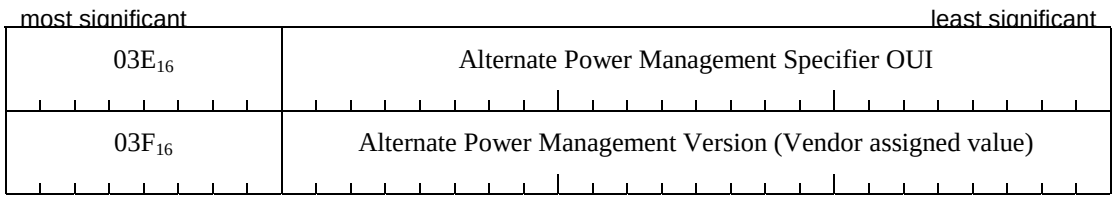

Figure 8-15 Alternate Power Management Specifier OUI and Version Entries

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9. Message Packets

A PDMS compliant node shall support DEP message request/response packet protocol.

This section describes the PDM message request and response formats used by PDMS compliant nodes.

9.1 General Message packet format

Message packets are a general purpose configuration status register (CSR) write transaction on serial bus.

A message request is a write transaction to the message request register in a node's CSR space (address FFFF F000 0080_{16}). The message request register is 64 bytes in size - that is, the message request register may be written with 64 bytes of data. However, 8 bytes of data are reserved for message packet header information, therefore, the actual data that can be written to the message request register is 56 bytes (14 quadlets).

A message response is a write transaction to the message response register in a node's CSR space (address FFFF F000 00C016). The message response register is 64 bytes in size - that is, the message response register may be written with 64 bytes of data. However, 8 bytes of data are reserved for message packet header information, therefore, the actual data that can be written to the message response register is 56 bytes (14 quadlets).

The following figures illustrate message request and message response packet format.

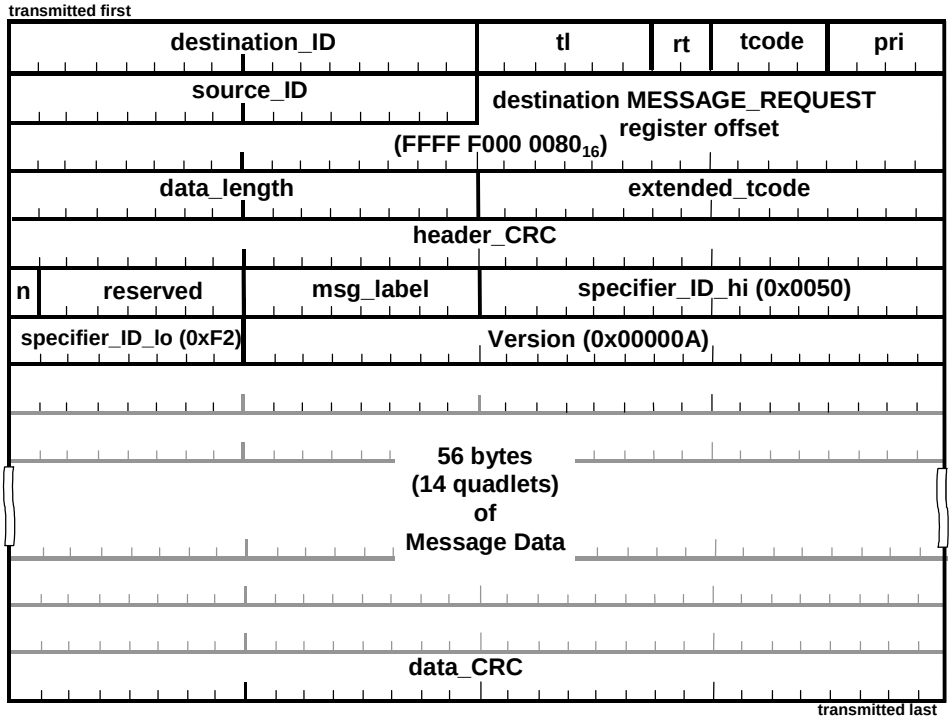

Figure 9-1 Message Request Packet Format

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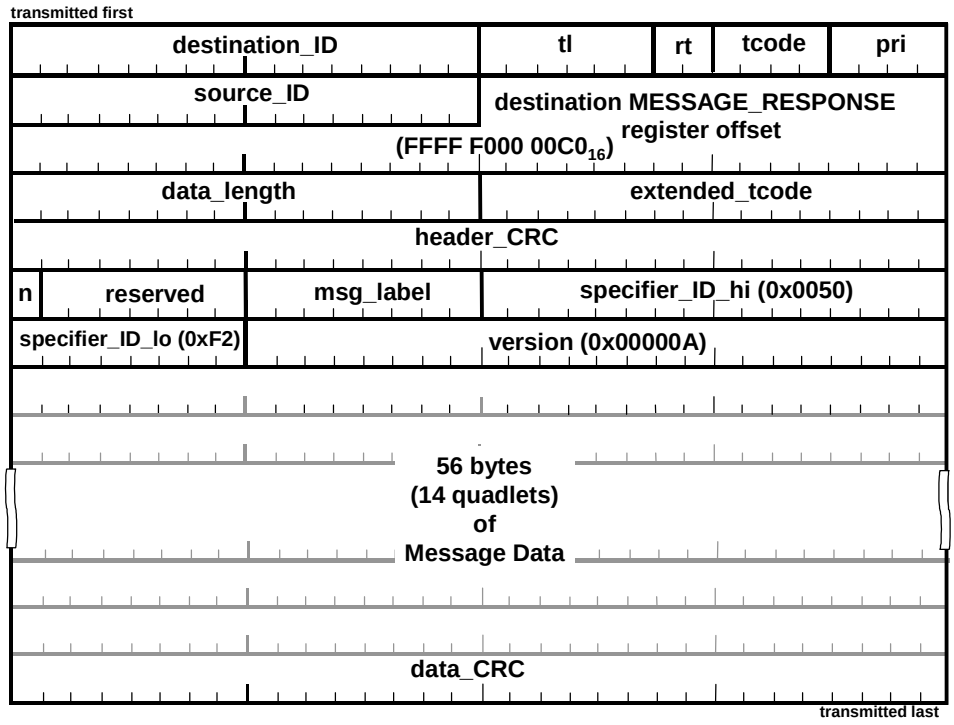

Figure 9-2 Message Response Packet Format

The usage of the *notify* bit (abbreviated as *n* in the preceding figures) depends upon its context. When a message is written to the message request register and *notify* is one, a response shall be written to the requester's message response register upon disposition of the request. Otherwise, when *notify* is zero, the requester indicates that no response shall be returned. When a message is written to the message response register and the *notify* bit is one, the request has been refused by the recipient because it is unrecognized, in which case the data written to message response shall be identical to that received at message request. When a response is received with a zero *notify* bit, the request has been processed by an application and the success or failure of the request shall be indicated by information in the *message dat*a.

The *msg_label* field permits the requester to correlate a response written to message response with an outstanding request. Despite the presence of the *msg_label* field, the message passing facilities of these two registers are, for all practical purposes, unconfirmed.

The 24-bit registration identifier *specifier_ID* and 16-bit *version* fields contain the values 0x0050F2 and 0x00000A, respectively – the specification identification and version of this specification - (see clause 7.1 if IEEE P1212, draft revision 1.0 dated October 18, 1999).

The values contained within the *message data* field are specified by their use in this specification.

When a message is written to the message response register, the value of the *msg_label*, *specifier_ID* and *version* fields shall be identical to their values written to the message request register when the request was received.

9.2 PDM_Message request format

A PDMS complaint node, when a change in its power requirements (either an increase or decrease) shall write a **PDM_Message** message to the write request register of the PDM.

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The PDM shall recognize a **PDM_Message** request register write initiated by a function proxy of a Legacy cable-powered node. A **PDM_Message** that has a message initiator node-ID unique from the cable-powered node ID shall be **PDM_Message** request generated by a proxy.

The following figure illustrates the **PDM_Message** request format.

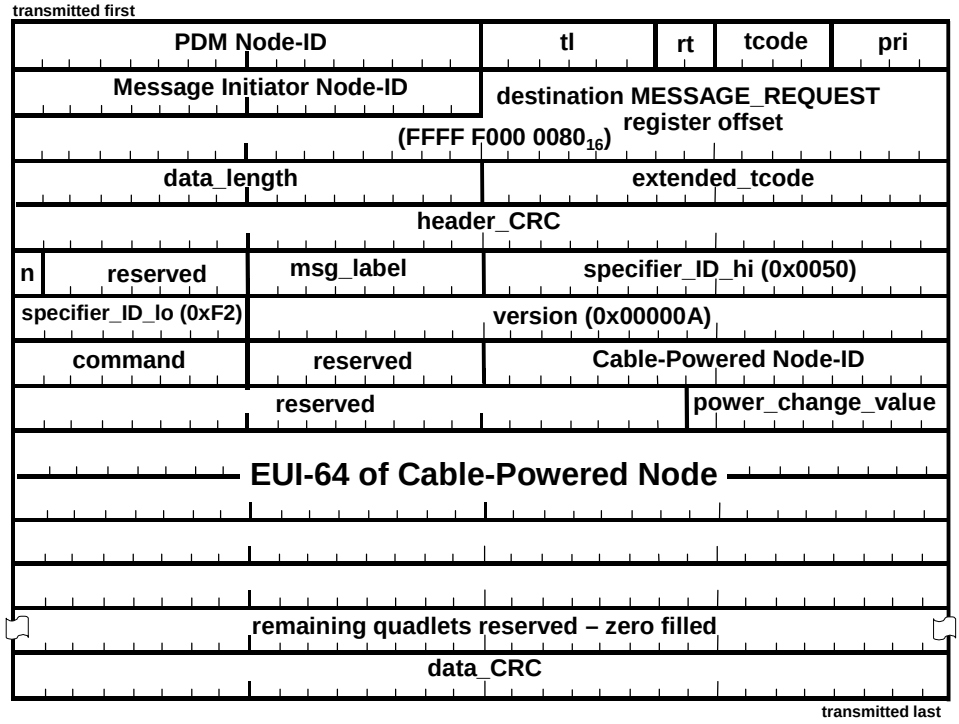

Figure 9-3 PDM message format

The *command* field determines the action to be taken by the message recipient as defined in the following table.

Table 9-1 *command* field values

command	ALLOCATION TYPE
00_{16}	Link Off, Maintain Node Power Allocation
01_{16}	Node Power Enable (Link on)
02_{16}	Deallocate request (lower) power
03_{16}	Allocate request (increase) power
04_{16}	Link Off, Release Node Power Allocation, Maintain PHY power allocation
05_{16}	Node Power Source Status Request
06_{16}-FF_{16}	Reserved

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The field *power_change_value* defines the amount of change in allocated node power (in deciwatts) .

A deallocation request does not require a response (*notify* shall be 0 in the message request). A request message for an increase in power allocation requires a message response from PDM (*notify* shall be one in the message request). When there is insufficient power in the power domain to satisfy the request for a power allocation increase, PDM shall write a message to the message response register of the initiator of the **PDM_Message** with an error code value of 01_{16}.

The *Cable-Powered Node-ID* field contains the 16-bit node-ID of the cable-powered node that the **PDM_Message** references.

The *EUI-64 of Cable-Powered Node* field contains the 64-bit EUI-64 of the cable-powered node that the **PDM_Message** references.

9.3 PDM_Message response

The format for a response to a **PDM_Message** request is illustrated in the following figure:

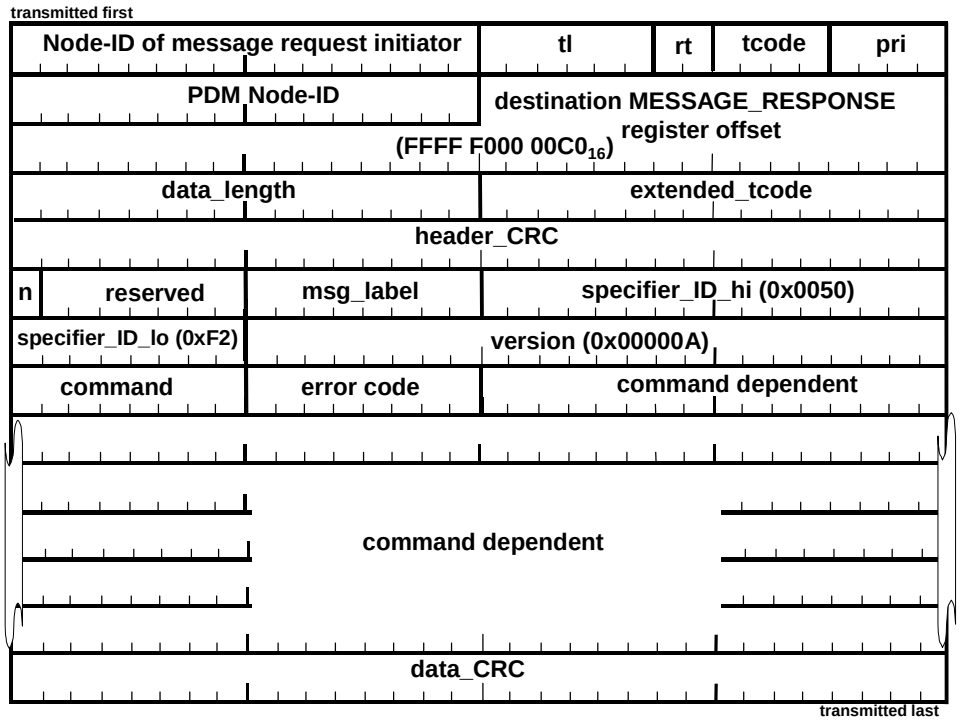

Figure 9-4 PDM_Message response format

The *command* field is the same value as that in the *command* field of the **PDM_Message** request.

The *command dependent* data fields contain information specific to the command processed by the PDM. This data is defined is subsequent sections of this specification.

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The error code returned shall be one of the error code values in the following table:

Table 9-2 *error code* field values

error code	DESCRIPTION
00_{16}	No error
01_{16}	Insufficient power available
02_{16}	Illegal Command
03_{16}	Illegal Parameters
04_{16}-FF_{16}	Reserved

9.3.1 Link Off, Maintain Node Power Allocation

The PDM does not generate a response to command 00_{16}, "Link Off, Maintain Node Power Allocation". The initiator of command 00_{16}, "Link Off, Maintain Node Power Allocation" shall set the *notify* bit to 0.

The PDM may maintain an index of cable-powered nodes that have power allocated to them but have their link turned off.

9.3.2 Node Power Enable (Link On)

A message request command 01_{16}, "Node Power Enable" (Link on) may be sent to the PDM. Upon receipt of this command, PDM may enable the identified node's link.

When known, the cable-powered node-ID and the EUI-64 shall be contained in the **cable-powered Node-ID** and **EUI-64 of Cable-Powered Node** fields, respectively, of the message request packet.

When power has been previously allocated to the cable-powered node, the PDM will send a link on PHY configuration packet to the node.

The PDM will respond with a write to the message response register of the message request initiator with an appropriate value in the error code field.

An error code value of 00_{16} informs the message request initiator that the link of the cable-powered node has been turned on and that the cable-powered node has responded with a ping packet addressed to itself – the cable-powered node is ready to respond to serial bus transaction packets. The 16 bits of command dependent data following the error code field shall contain the node-ID of the cable-powered node. The EUI-64 of the cable-powered node follows the cable-powered node-ID.

When power has not been previously allocated to the cable-powered node, the PDM will determine if there is sufficient power in the power domain that would allow the link to be enabled. If there is insufficient power, the PDM will respond to the message request initiator by writing to the message request register of the initiator with an error code value of 01_{16} – Insufficient Power Available.

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9.3.3 Deallocate Request (lower) Power

When the PDM receives command 02_{16}, "Deallocate request (lower) power", the PDM reduces the amount of power allocated to the cable-powered node by an amount equal to the value contained in the power_change_value field of the message request packet.

The amount of power deallocated from the cable-powered node is returned to the power domain power available pool.

Prior to updating the contents of the Node_Power register, the PDM shall read the Node_Power_Required register and validate the new value to be written to the Node_Power register against the value in the Node_Power_Required register. When the values do not correlate, the PDM shall respond to the message request initiator with a write to the message response register of the initiator with an error_code field value of 03_{16} – "Illegal Parameters".

The PDM shall respond with a write to the message response register of the message request initiator with an error code field value of 00_{16} (no error) after successfully updating the value in the Node_Power register of the cable-powered node.

9.3.4 Allocate Request (increase) Power

When the PDM receives command 03_{16}, "Allocate request (increase) power", the PDM increases the amount of power allocated to the cable-powered node by an amount equal to the value contained in the power_change_value field of the message request packet.

The amount of additional power allocated to the cable-powered node shall be deallocated from the amount of available power in the power domain of the cable-powered node.

Prior to updating the contents of the Node_Power register, the PDM shall read the Node_Power_Required register and validate the new value to be written to the Node_Power register against the value in the Node_Power_Required register. When the values do not correlate, the PDM shall respond to the message request initiator with a write to the message response register of the initiator with an error_code field value of 03_{16} – "Illegal Parameters".

Before updating the contents of the Node_Power register, the PDM shall determine if there is sufficient power available in the power domain of the cable-powered node to allocate to the cable-powered node. When there is insufficient power available in the power domain, the PDM will respond to the message request initiator by writing to the message request register of the initiator with an error code value of 01_{16} – Insufficient Power Available.

The PDM shall respond with a write to the message response register of the message request initiator with an error code field value of 00_{16} (no error) after successfully updated the value in the Node_Power register of the cable-powered node.

9.3.5 Link Off, Release Node Power Allocation, Maintain PHY Power Allocation

The PDM does not generate a response to command 04_{16} - "Link Off, Release Node Power Allocation, Maintain PHY power allocation" command. The initiator of command 04_{16} shall set the *notify* bit to 0.

The amount of power deallocated from the cable-powered node is returned to the power domain power available pool.

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9.3.6 Node Power Source Status Request

The PDM shall determine the amount of power being delivered through individual ports on the power provider by sending a message request command 05_{16}, "Node Power Source Status Request" to the power provider in a power domain. The power provider responds with a write to the PDM message response register with command data field containing power delivery status for each port (up to sixteen ports). Nine bits are used to identify the number of deciwatts being delivered out a port. The first four bits of the command data response field identify the number of ports implemented. There shall be one nine-bit power value for each implemented port. Ports that are either not implemented or do not have power being delivered through them shall have their data set to zero. The command data response field shall be filled with zeros after the last valid port entry.

The format for a response to a **"**Node Power Source Status Request" message request is illustrated in the following figure:

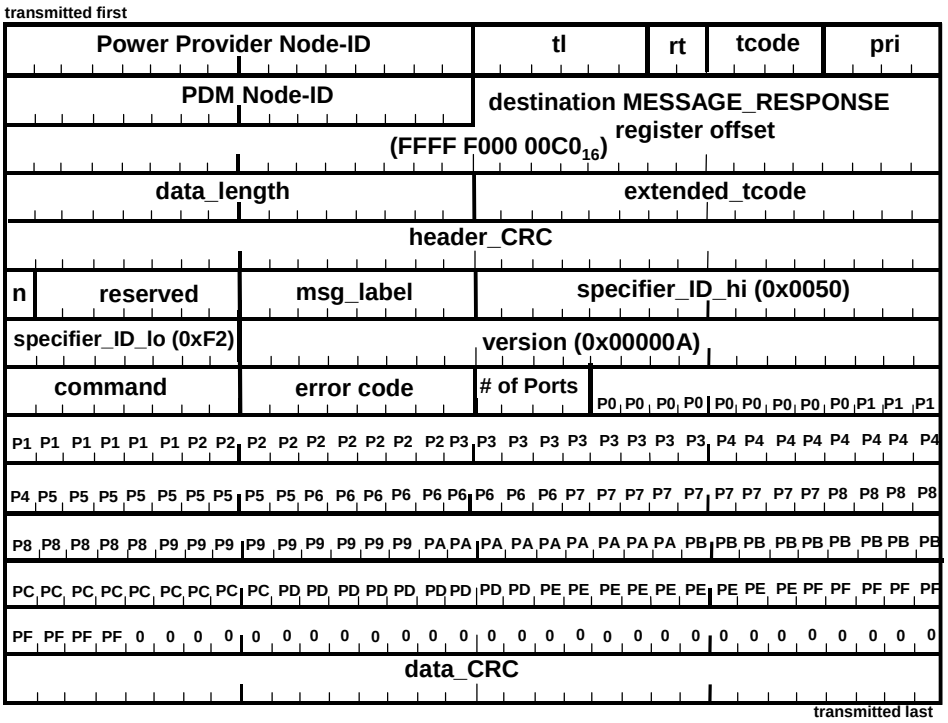

Figure 9-5 "Node Power Source Status Request" message response

The *command* field is the same value as that in the *command* field of the message request from the PDM.

The amount of power, in deciwatts, delivered to the serial bus from a port in the power provider is contained in a nine-bit value for the identified port in the above figure. The port is identified by the P*n* in the above figure where *n* is the port number in the range of 0_{16} to F_{16}.

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Annexes

Annex A: Low Power States and Wake Events(normative)

A.1 Establishing Power Policy Client/Owner

A power consumer may be placed in a low power consumption state. Once in a low power state, it may generate a wake event. While a cable-powered node is in a low power state, the power policy owner for the node may generate a wake event.

Message request and message response mechanisms shall be used between a cable-powered node and its prospective power state policy owner to establish a client/owner relationship. Data field contents for message request/response packets used to establish a client/owner relationship between two nodes are beyond the scope of this specification but shall be understood between the power policy owner and its prospective cable-powered client.

Once a client/owner relationship has been established, the client and its power policy owner node shall use the protocol set forth in this annex.

A.2 Initiating Cable-Powered Node Power State Transitions

The power policy owner for a cable-powered node defines when and under what conditions a client cable-powered node shall alter its power consumption state. The power policy owner may transmit a message request packet to the cable-powered node instructing the node to change its power state. The values contained in the data field for a power state change message request packet are beyond the scope of this specification but shall be understood between the power policy owner and its cable-powered client.

A client cable-powered node may initiate its own power state transition – dependent upon the established policy between itself and its owner.

Prior to initiating a power state transition, a client cable-powered node shall write a message request containing power state transition information in the data field to the message request register of its owner. This message requires a response from the owner. The response shall be an affirmation (grant) to the client to initiate the change or a request denied response.

The details of the message request/response protocol between the client and its owner are beyond the scope of this specification but shall be known between the client and the owner.

A.3 Cable-Powered Node Power State Transition Actions

Upon receipt of a power state transition message request from its owner, a client cable-powered node shall change its power consumption state to the state specified by its owner.

When the power state transition results in the link of the cable-powered node to be disabled while power allocated to the node is to be maintained, the cable-powered node shall write a message request command 00_{16}, “Link Off, Maintain Node Power Allocation” to the PDM write request register.

When the power state transition results in the link of the cable-powered node to be disabled and power allocated to the node is no longer required, the cable-powered node shall write a message request command

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04_{16}, "Link Off, Release Node Power Allocation, Maintain PHY power allocation" to the PDM write request register.

A cable-powered node that has transmitted a "Link Off, Maintain Node Power Allocation" message request command to the PDM may enable its link at anytime - without regard as to whether it has received a link on PHY configuration packet from the PDM. When a cable-powered node enables its link when returning from a low power conservation state, the cable-powered node shall transmit a ping packet addressed to its own node-ID. When the PDM receives the ping packet from the cable-powered node, the PDM may make use of this information as notification that the cable powered node's link is enabled.

After sending its ping packet, the cable-powered node may use a message request packet to communicate to its power policy owner node information specific to the cable-powered node wake event. The node-ID of the power policy owner may have changed, therefore, the cable-powered node may discover the node-ID of its power policy owner via the use of a DEP message request packet containing the EUI-64 of the power policy owner.

A.4 Power Policy Owner Power State Transition Actions

The power policy owner of a cable-powered node may send a message request command 01_{16}, ("Node Power Enable") to the PDM to enable the link of a cable-powered node.

The power policy owner may use, upon receiving the ping packet the cable-powered node transmitted to itself as a response to the link on, a message request packet to communicate to the cable-powered node information specific to the power policy owner generated wake event. Alternatively, the power policy owner, being the initiator of the "Node Power Enable" message request command to the PDM, may wait until the response is received from the PDM – the response will contain the node-ID and EUI-64 of the cable-powered node.

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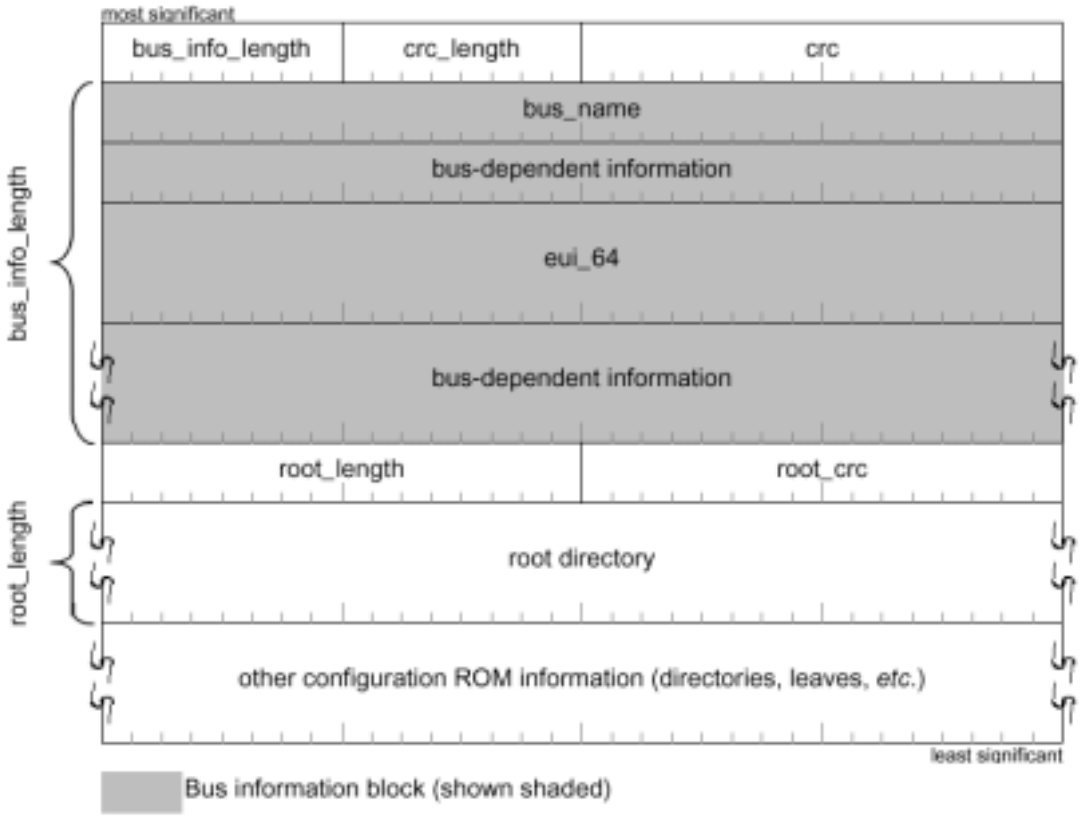
Annex B: Configuration ROM Example (informative)

B.1 Node Configuration ROM

The first quadlet of general format configuration ROM, the bus information block and the root directory are all at predetermined offsets from FFFF F000 040$_{016}$ while all other data structures—directories, leaves and vendor-dependent information—may occur at any address after the fixed elements. The structure of general format configuration ROM is shown by the following figure.



Annex A- 1 General ROM format

The bus information block has been described in clause 8.1.

The root directory occurs at the offset FFFF F000 040$_{016}$ + 4 *(bus_info_length* + 1), immediately following the bus information block. The format of the root directory is the same as all other directories; the contents of the root directory are described in more detail in clause 7.6.1 of IEEE P1212 (draft 1.0). Directory entry format can be reviewed in clause 7.2 of this specification. The root directory contains entries for `PDM_Registers` and `Node_Power_Directory`.

The contiguous block of configuration ROM that starts immediately after the end of the root directory is available for directories, leaves and vendor-dependent information. These data structures may appear in any order; they form a hierarchical tree accessed by means of relative address pointers as described in clause 7.7.18 of IEEE P1212 (draft 1.0). It is here where data entries for the `Node_Power_Directory` are located.

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